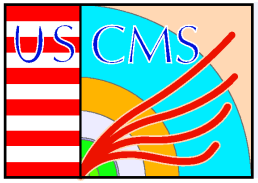


US CMS TriDAS

US CMS Meeting

Wesley H. Smith, *U. Wisconsin*
CMS Trigger Project Manager

May 10, 2002

Outline:

Calorimeter Trigger Status & Plans

Muon Trigger Status & Plans

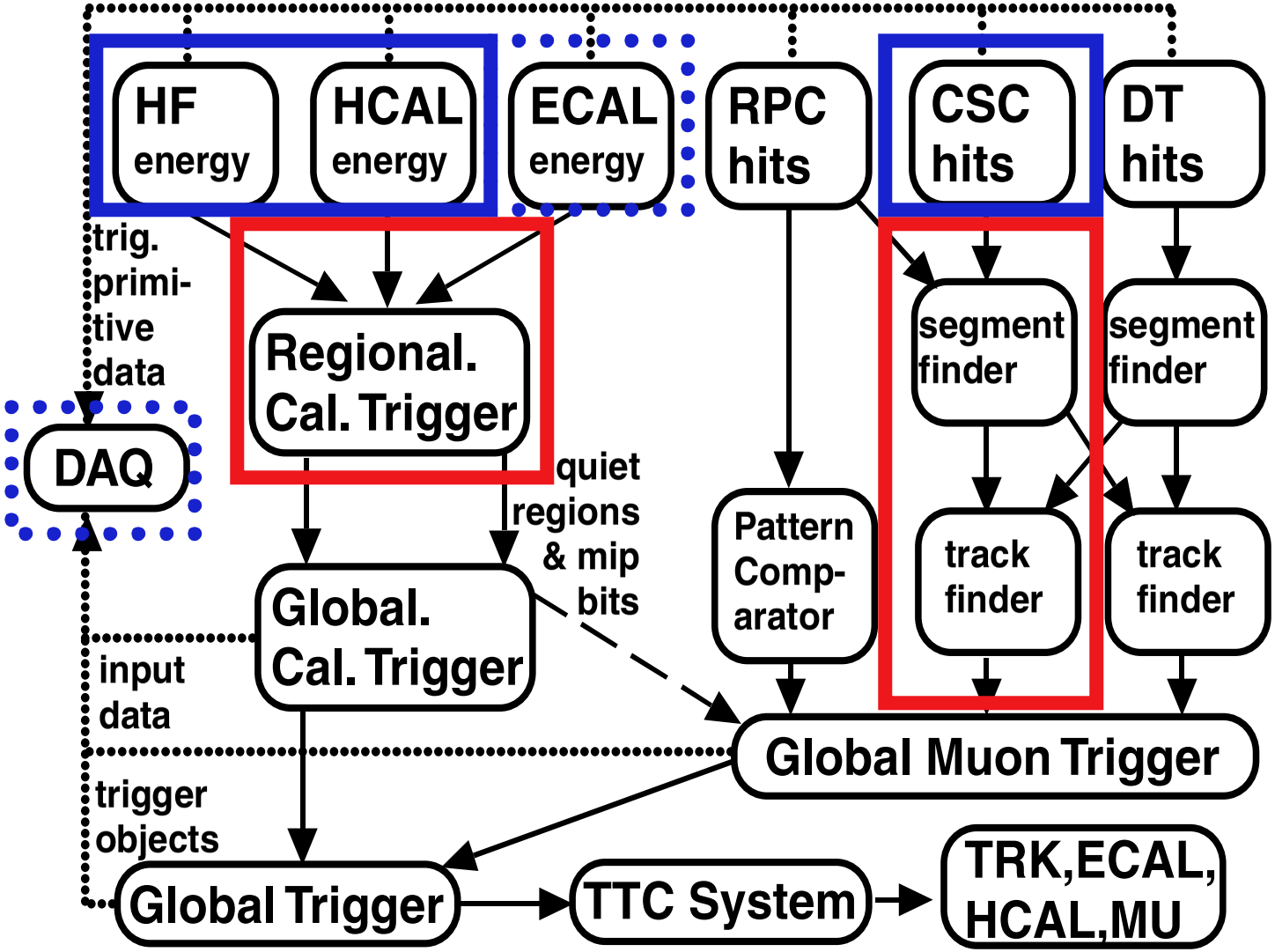
DAQ Status & Plans (from Vivian O'Dell)

This talk is available on:
http://hep.wisc.edu/wsmith/cms/TriDAS_USCMS_0502.pdf

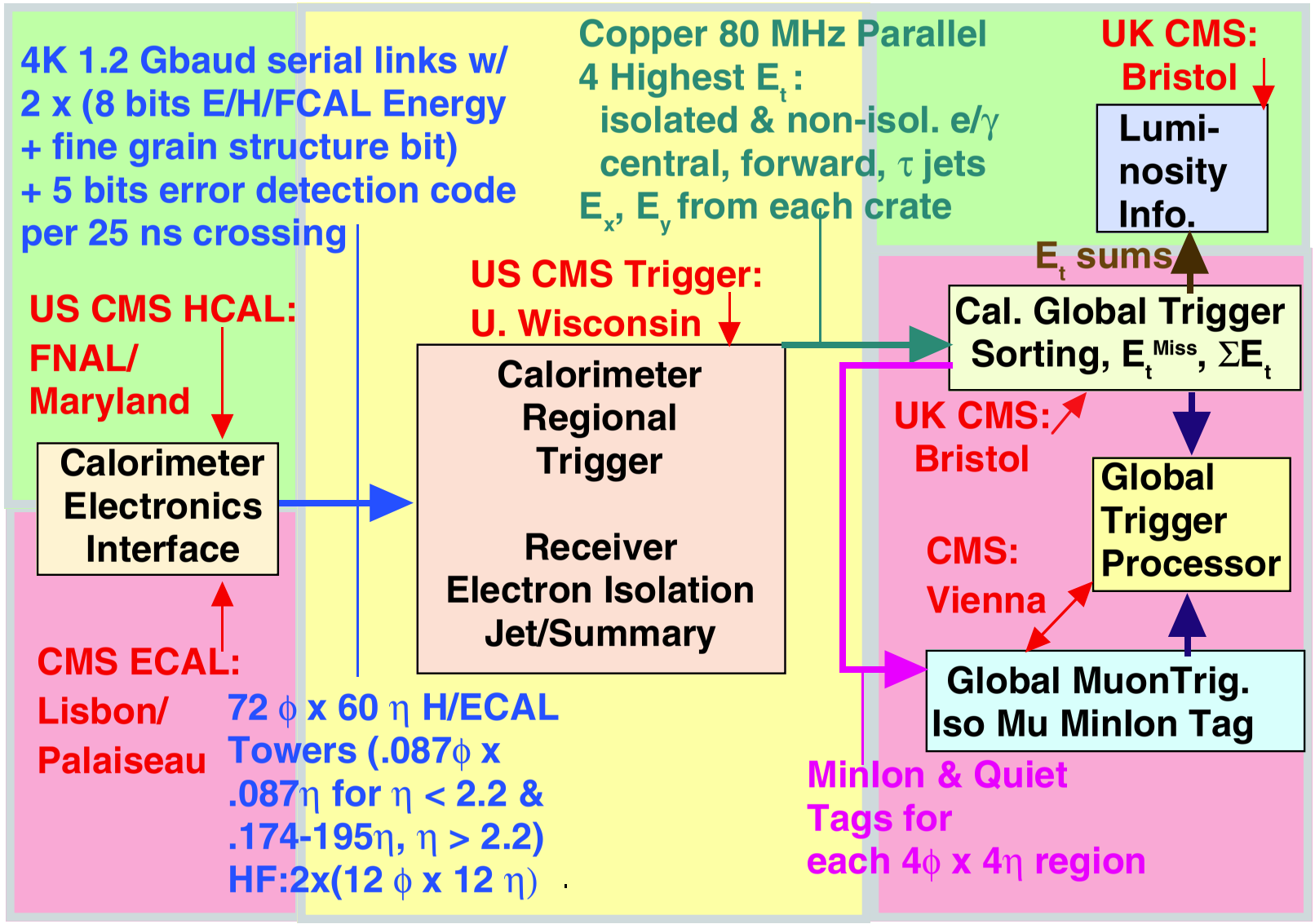
L1 Trigger Hardware Overview

US CMS Trigger (this talk)

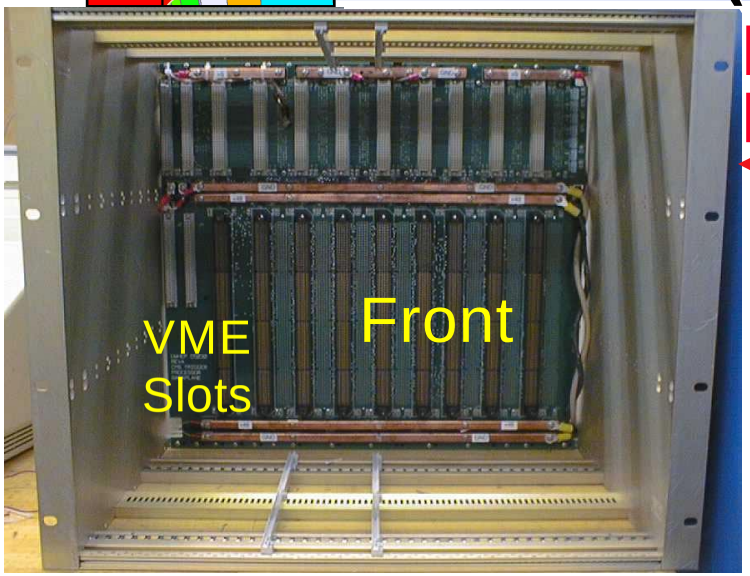
US CMS

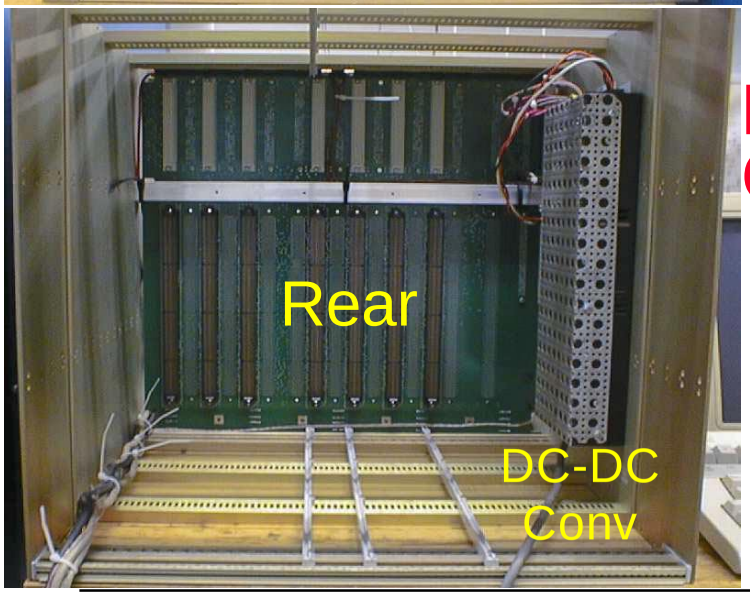


Calorimeter Trig.Overview



Cal. Trig 2nd Gen. Prototypes (U. Wisconsin)



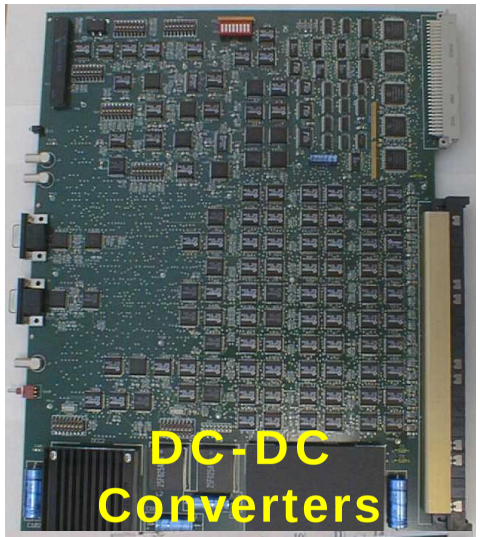


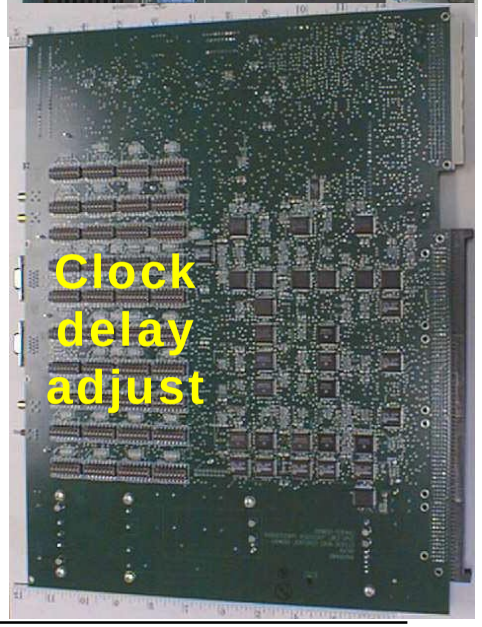
New High-Speed Backplane

- 160 MHz with 0.4 Tbit/sec dataflow
- Designed to incorporate algorithm changes
  - New Non-Isolated Electron, Tau & Jet Triggers

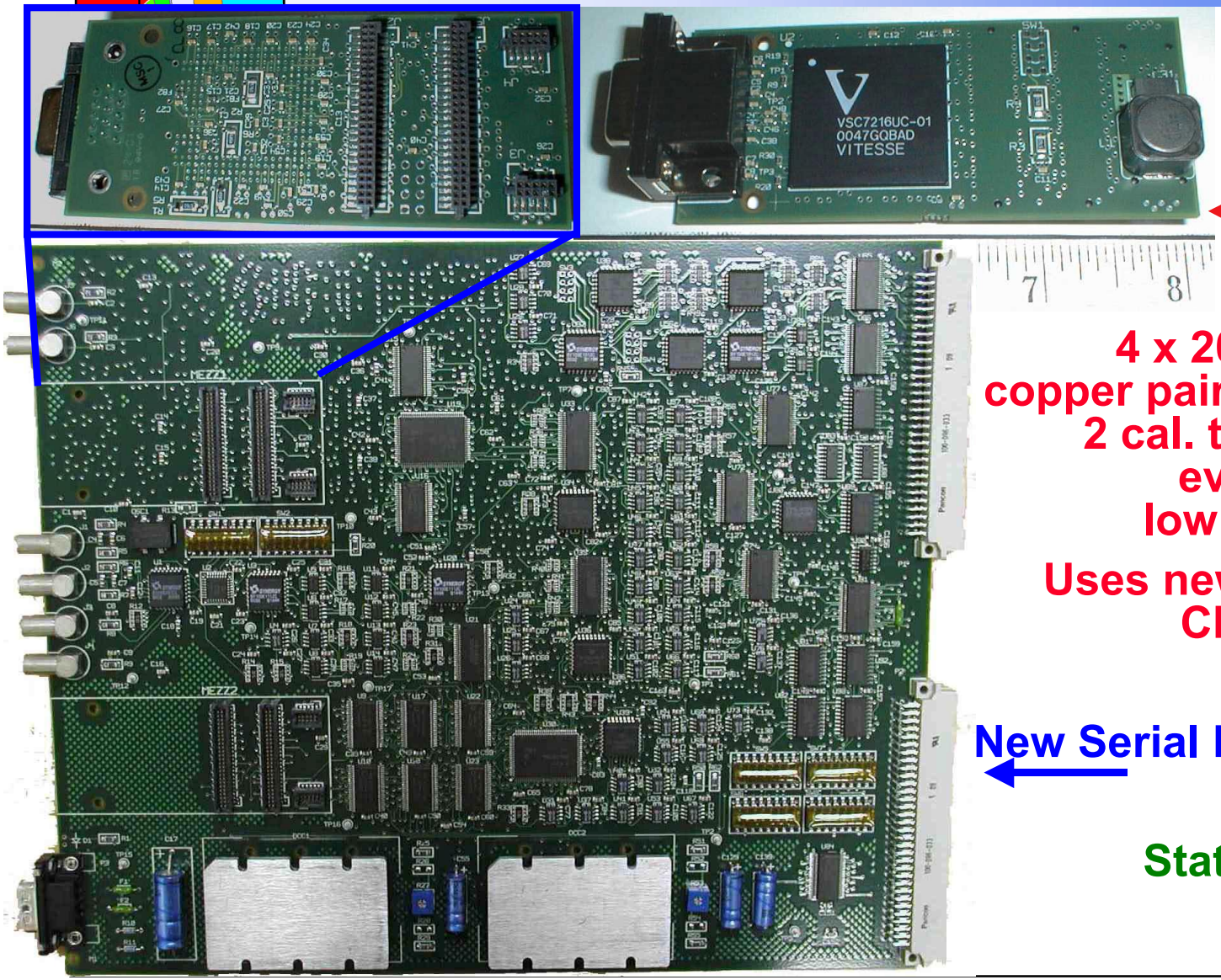
New Clock & Control Card

- Fans out 160 MHz clock & adjusts phases for all boards
  - 50% tested successfully





New Cal. Trig. 4 Gbaud Copper Link Cards & Tester (U. Wisconsin)



8 Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power.

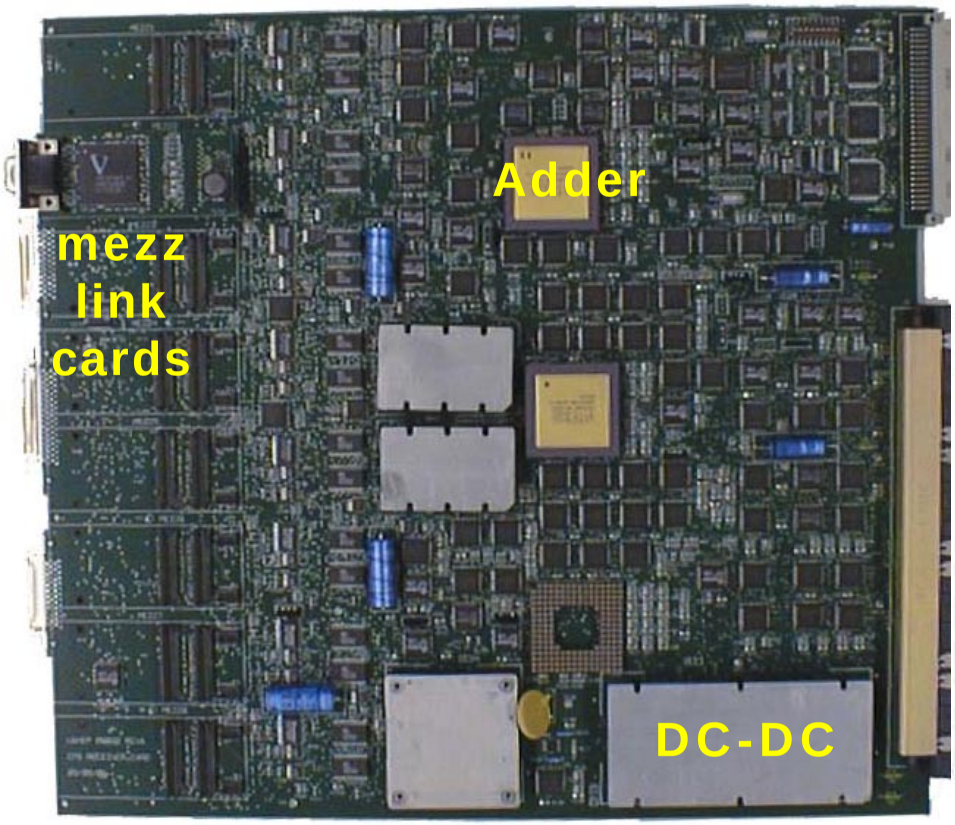
Uses new Vitesse Link Chips (7216-01).

New Serial Link Test Card

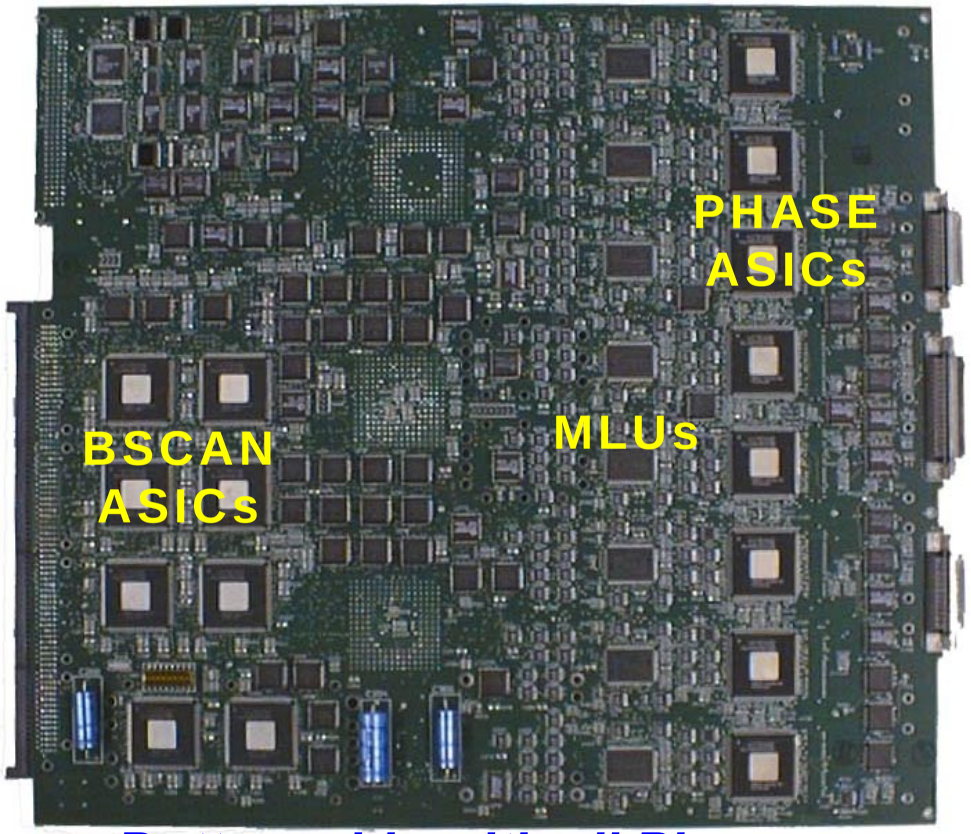
Status: under test

New Calorimeter Trigger Receiver Card (U. Wisconsin)

Full featured final prototype board is in test - initial results are good.
Continue to test on-board ASICs & copper link mezzanine cards

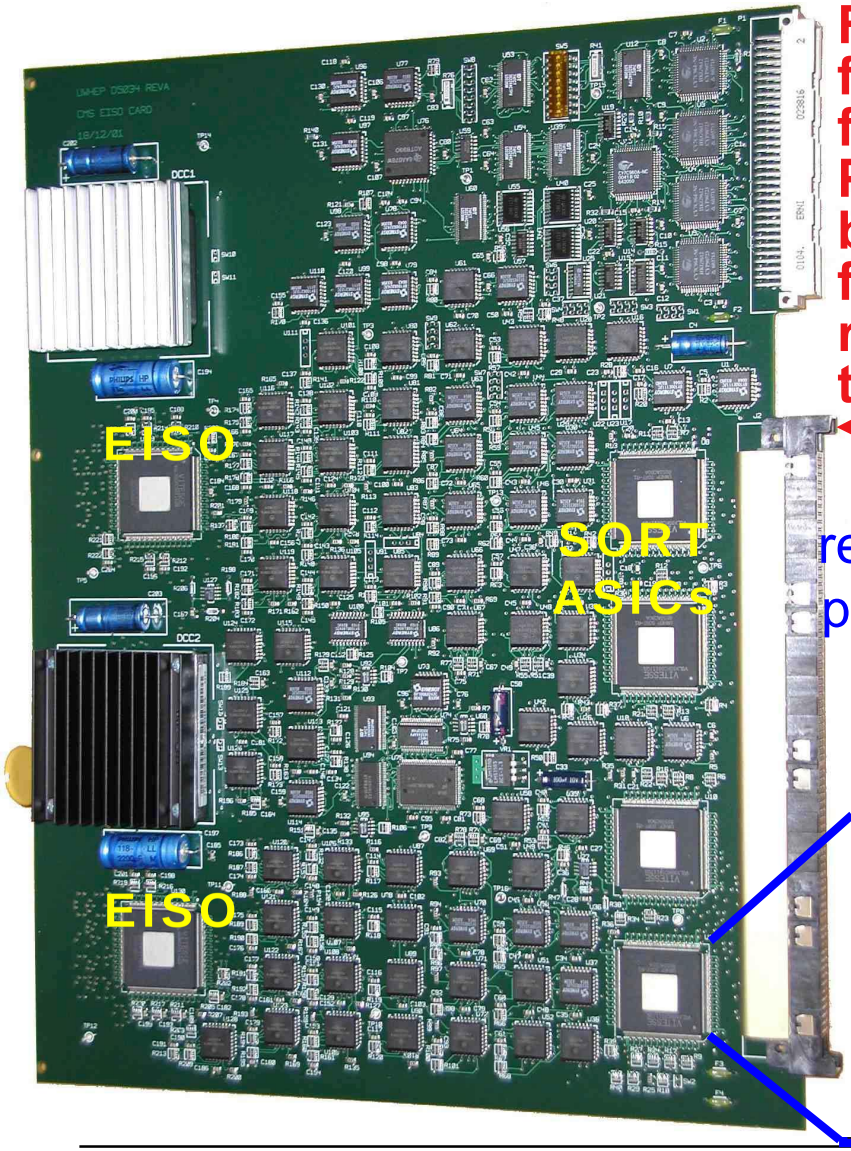


Top side with 1 of 8 mezzanine cards & 2 of 3 Adder ASICs



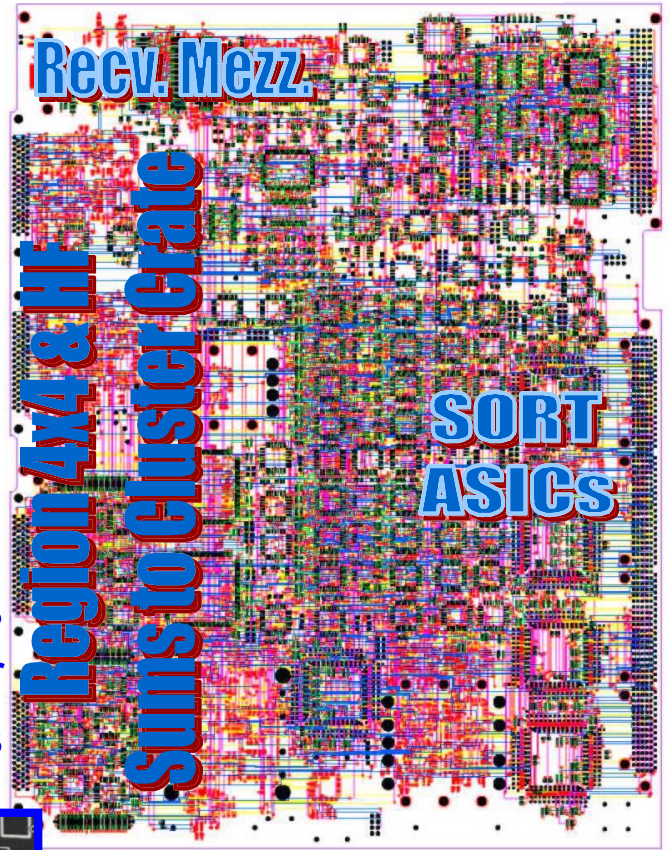
Bottom side with all Phase & Boundary Scan ASICs

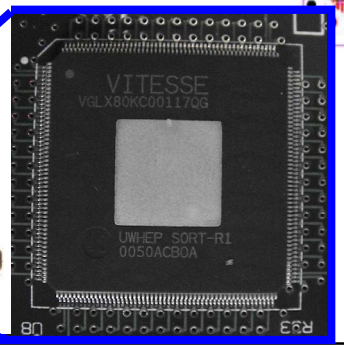
Cal. Trig. New Electron Isolation & Jet/Summary Cards (Wisconsin)



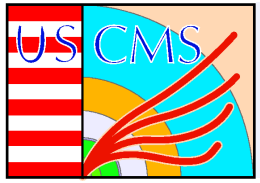
Full featured final E.I. Proto. board is finished & ready for testing.

JSC Proto. ready to build pending tests of other boards





E.I. Proto will test Electron Isolation ASICs & Sort ASICs



Cal Trigger Status/Plans

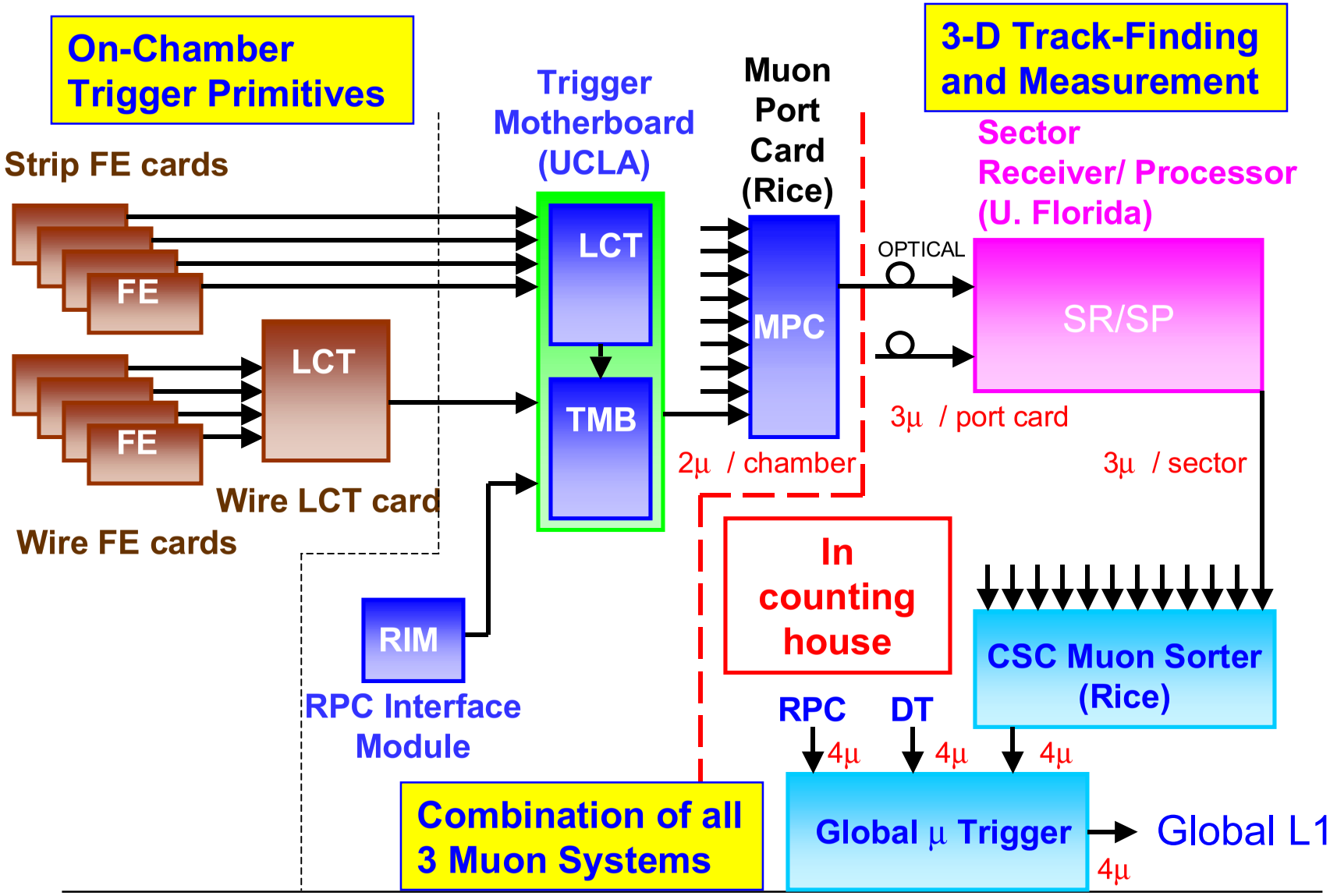
Preparing second generation prototype tests

- Crate, Backplane, Clock & Control, ASICs done
- Receiver Card & Electron Isolation Card ready.
- Serial Link Mezzanine Card Receiver done,
  Tester Card at vendor, Transmitter Tester in design

Goals for 2002

- Complete of prototype tests, validate ASICs
- Integrate Serial Links w/ECAL,HCAL front-ends
- Prototype Jet/Summary card manufacture
  - Ready for manufacture -- waiting for other board tests
- Finalize Jet Cluster crate design

CSC Muon Trigger Scheme



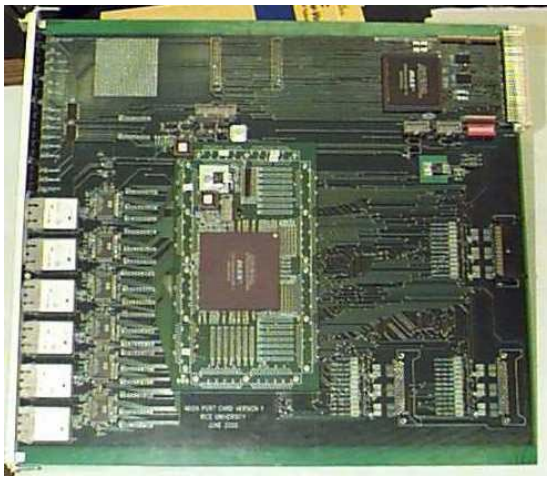
1st Muon Trigger Prototypes (Florida, Rice, UCLA)

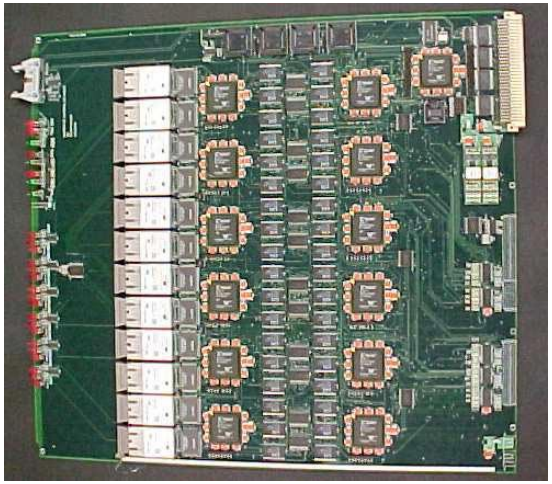
Successful CSC Trigger Integration test

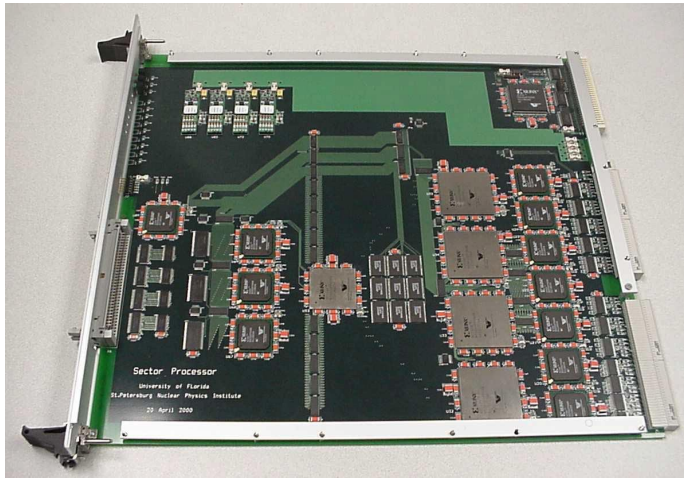
- Prototype Muon Port Card, Sector Receiver, Sector Processor, Clock Board, Backplane work & communicate -- Result in 2000

ORCA full simulation working

- Agreement/use with hardware test







1st Track-Finder Crate Tests

Sector Processor (Florida)

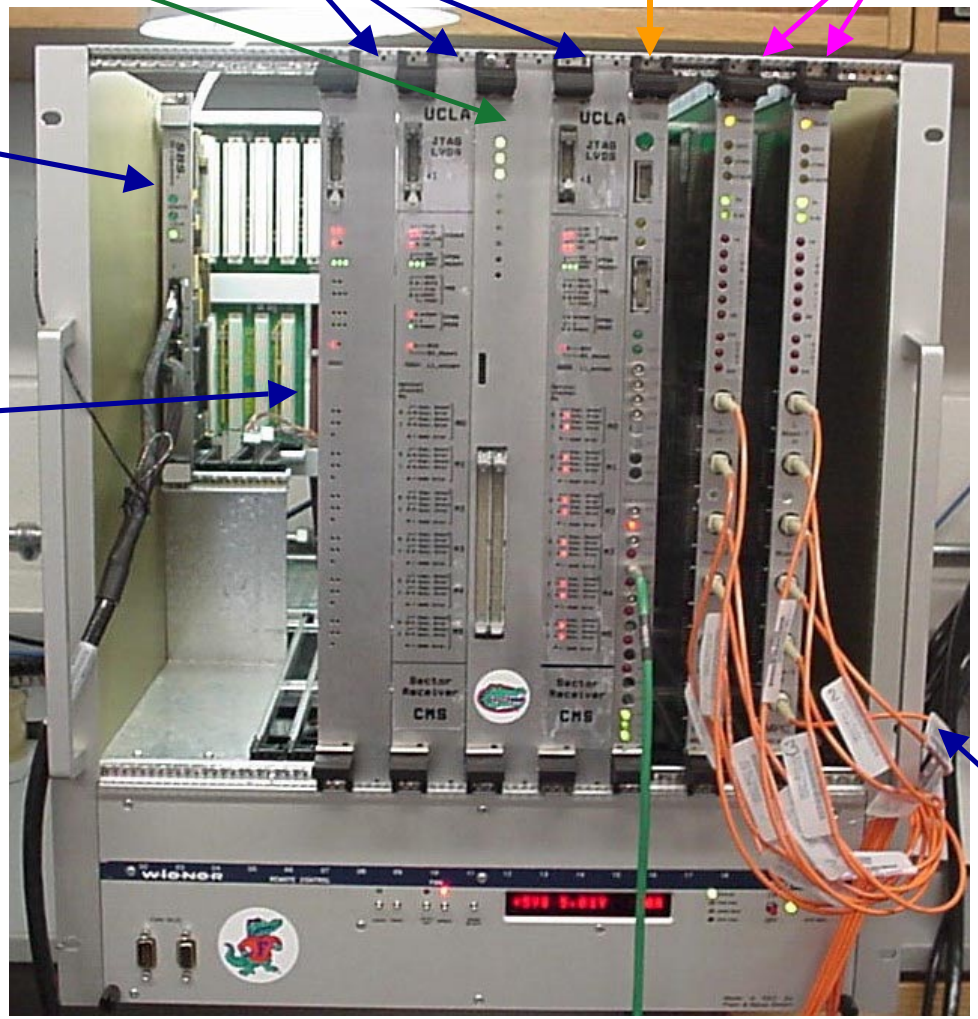
Sector Receiver (UCLA)

Clock Control Board (Rice)

Muon Port Card (Rice)

Bit3 VME Interface

Custom Backplane (Florida)



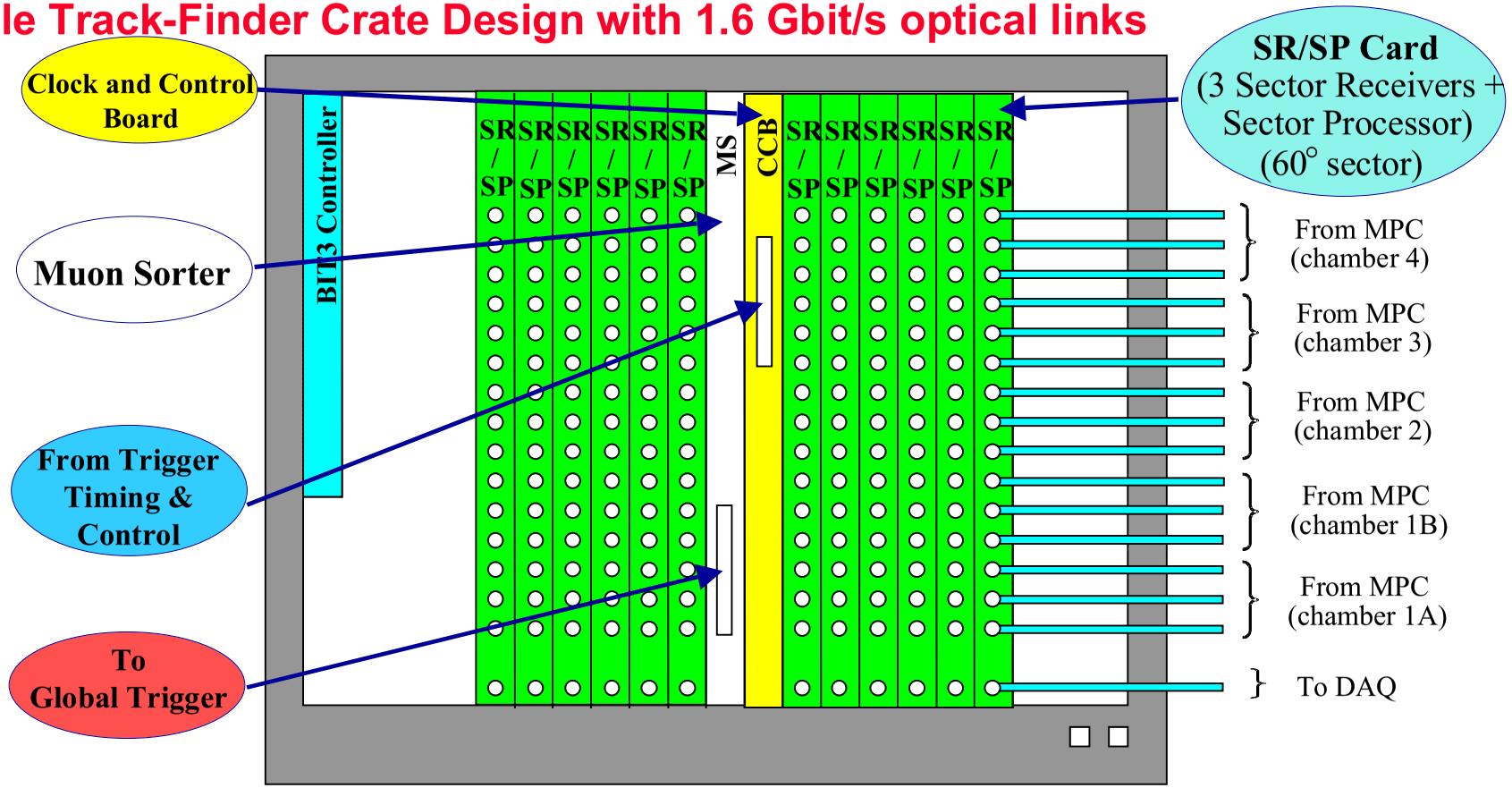
Prototype crate for original six crate design

Very successful but latency too high -- New design in 2001

100m optical fibers

New EMU Trigger Design: U. Florida Track-Finder

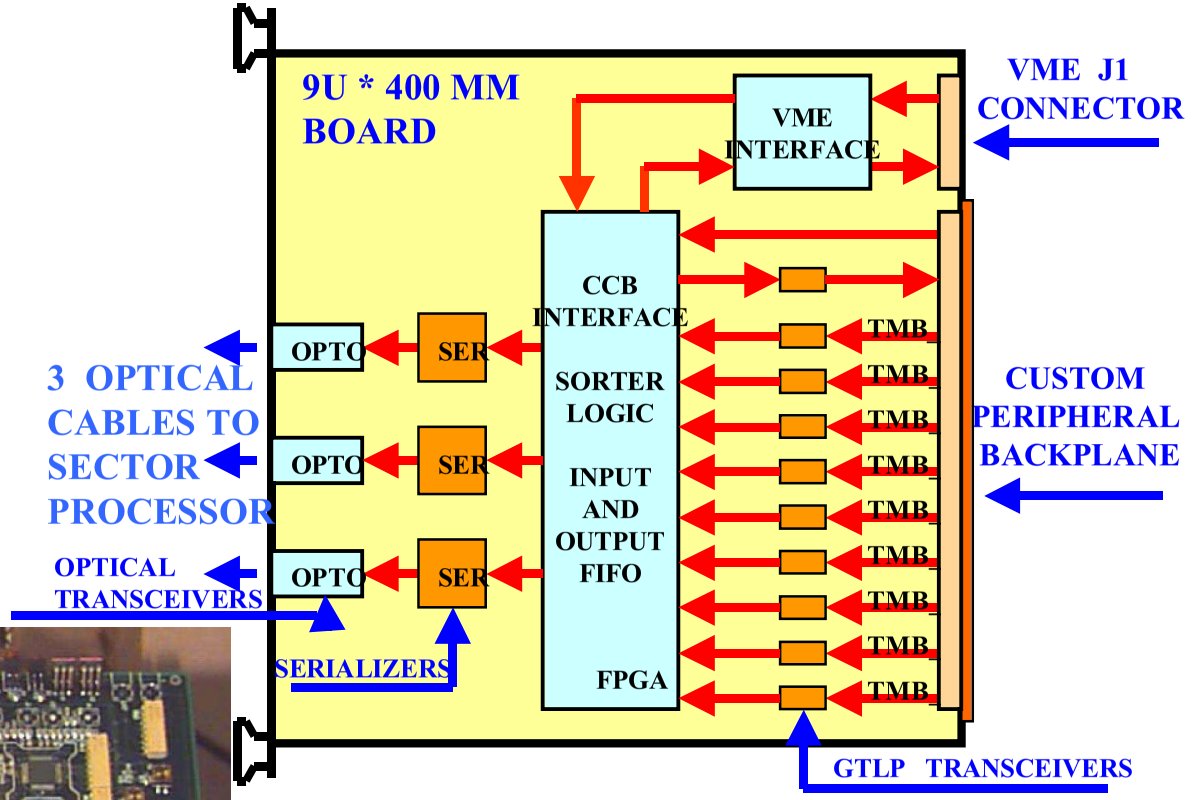
Single Track-Finder Crate Design with 1.6 Gbit/s optical links

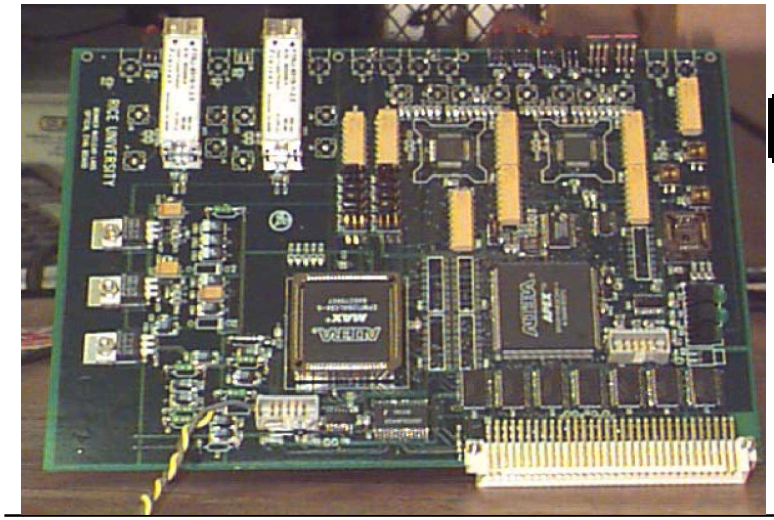


- **Reduces processing time from 525 ns (old design) to 175 ns**
  - Total Latency ~ 20 Bx (from input of SR/SP card to output of MS card)
- **Crate Power Consumption ~ 500 W • 15 Optical connections per SR/SP card**
- **Custom Backplane for SR/SP ⇔ CCB and MS connection**

New Muon Port Card Design & Optical Link Tests (Rice)

New MPC Design uses new high speed links (TLK2501) to send one muon per optical fiber
(needed for new compact track-finder design)





Optical Link Radiation Tests:
Three serializers: up to 270 kRad TID. No permanent damage or SEU
Two Finisar optical modules: No errors up to 70 kRad. Failed at 70kRad (well above ~10 kRad TID inner CSC dose for 10 years)

CSC Trigger Status/Plans

Prototype 1 tests now complete

Prototype 2 and production follow EMU components to optimize technology

MPC, SP, CCC modules, backplane* milestones:

- **Apr-02 Prototype 2 designs done**
  - Freeze CSC-DT interface
  - Determine DDU compatibility with OSU module for EMU
- **Nov-02 Prototype 2 construction done**
- **Apr-03 Prototype 2 testing done**
- **Sep-03 Final designs done**
- **Oct-04 Production done**
- **Apr-05 Installation done**

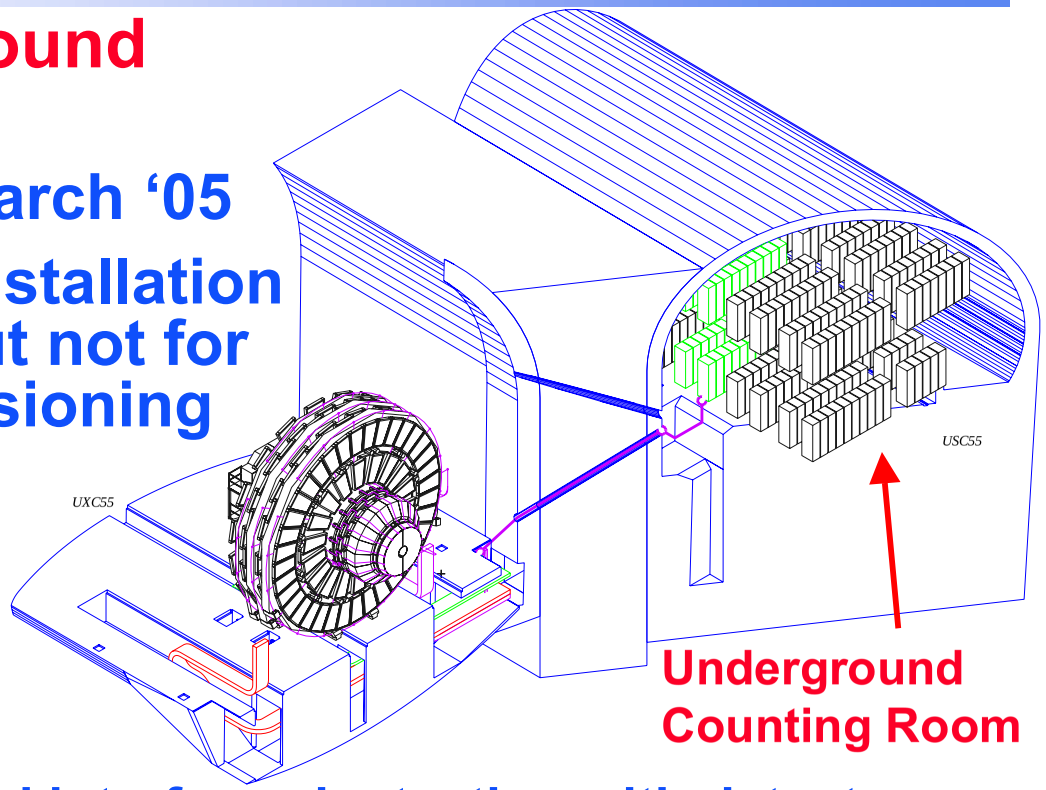
(*backplane schedule ~3 months ahead of above dates to provide platform for testing and integration)

Muon Sorter module: only 1, design by Jan-04

Schedule: Trigger Project Completion

Installation in Underground Counting Room

- Expect access by March '05
- Sufficient time for installation and some testing but not for completing commissioning with detectors



Slice Test (on surface)

With both HCAL and EMU

Verify trigger functions and interfaces by testing with detectors on surface at CERN.

Suggest as substitute for commissioning completion step.

Will check as much on surface before gaining access to underground facilities.

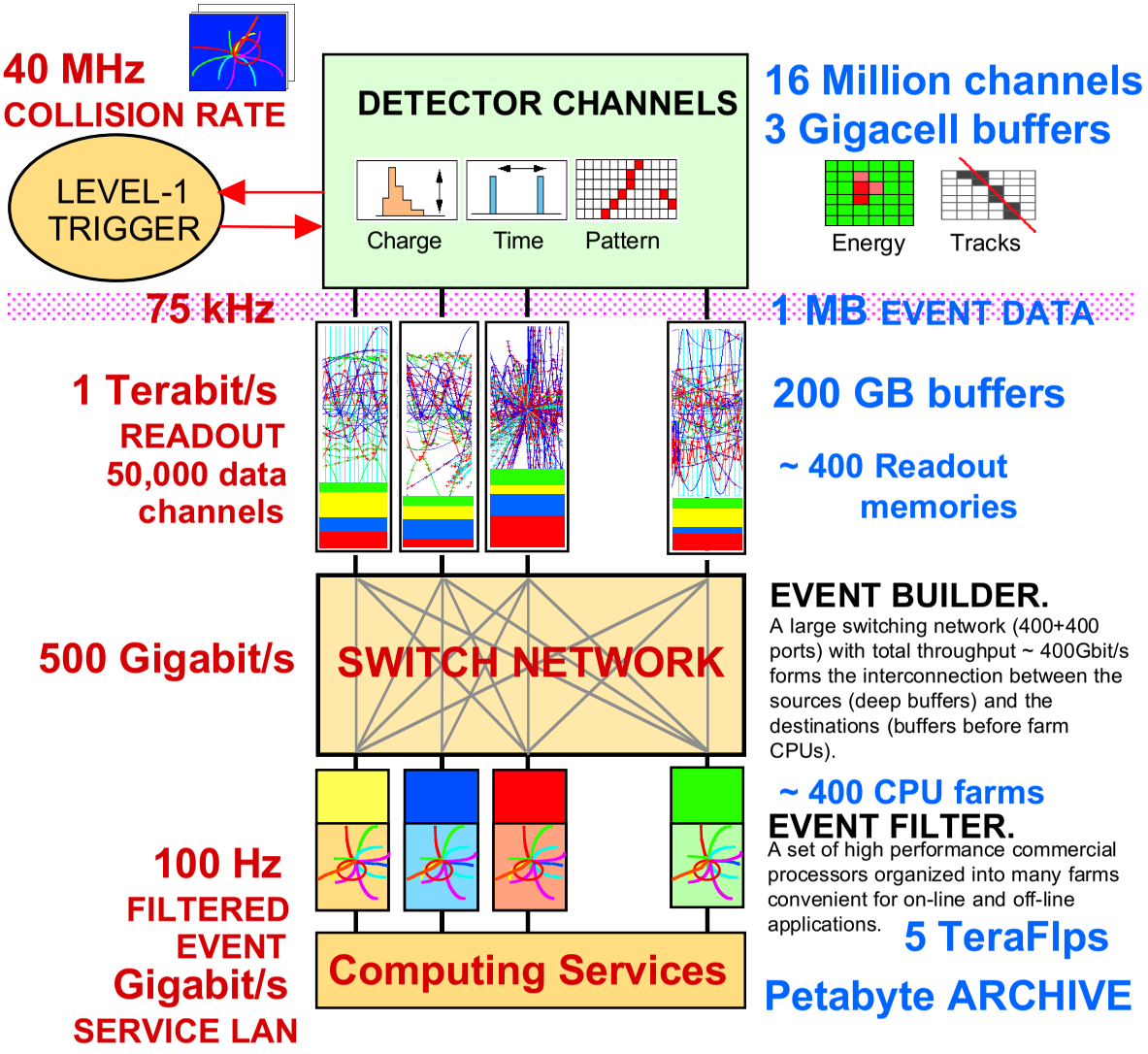
Planned for October '04 - March '05

Original Trigger L2 Task Schedule & Updates

Tasks	original start	finish	new
• Produce TDR	8/00	12/00	✔
• Design Final Prototypes	11/00	12/01	✔
• Construct Final Prototypes	6/01	6/02	⇒11/02
• Test/Integrate Final Prototypes	12/01	12/02	⇒ 4/03
• Pre-Production Design & Test	6/02	6/03	⇒11/03
• Production	12/02	6/04	
• Production Test	6/03	11/04	
• Trigger System Tests	5/04	5/05	
• "Slice Test" NEW ←	10/04	3/05	
• Trigger Installation	3/05	9/05	
• Integration & Test w/DAQ & FE	6/05	12/05	
• Maintenance & Operations	10/04	-------	

6 months civil engineering delay of installation date

DAQ System Overview



Original design:
L-1 @ 100 kHz

Rescope:
1997: 75kHz

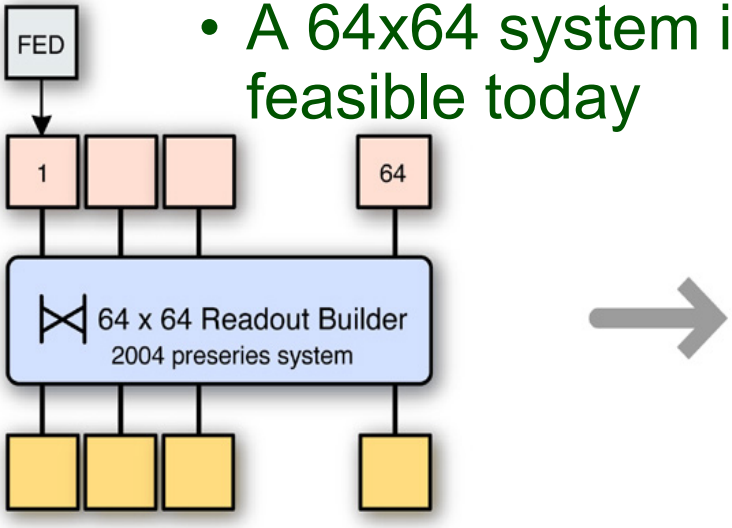
2001: Initial
L-1 @ 50 kHz

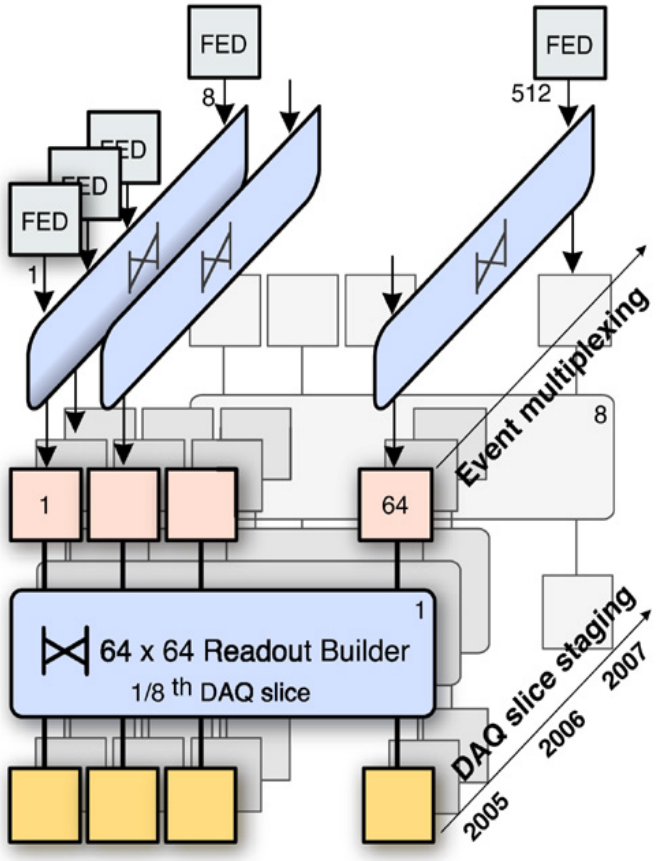
But design all elements to be able to do 100 kHz

New DAQ design: principle

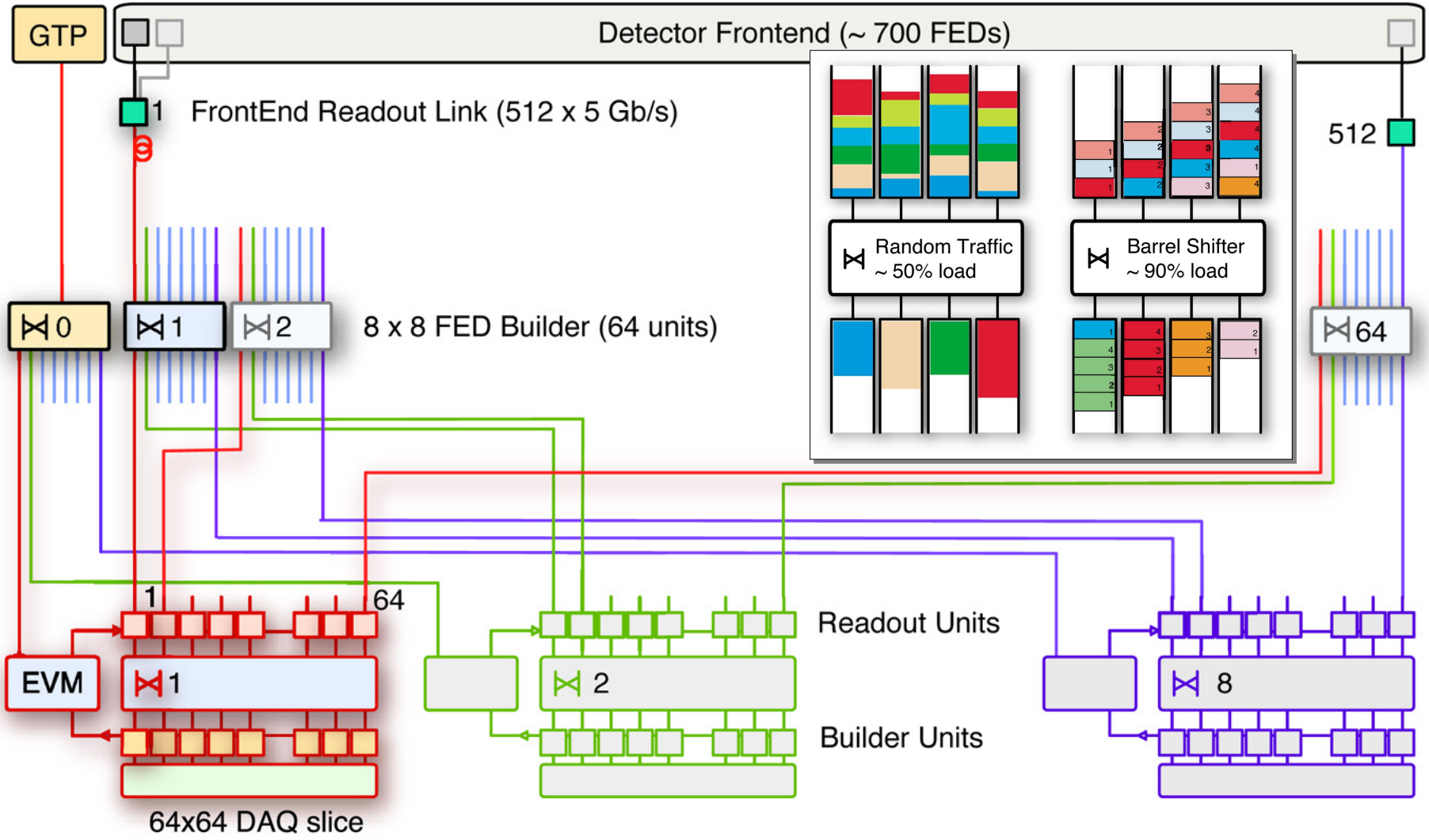
Basic principle:

- **Break DAQ into a number of functionally identical, parallel, smaller DAQ systems**
  - A 64x64 system is feasible today

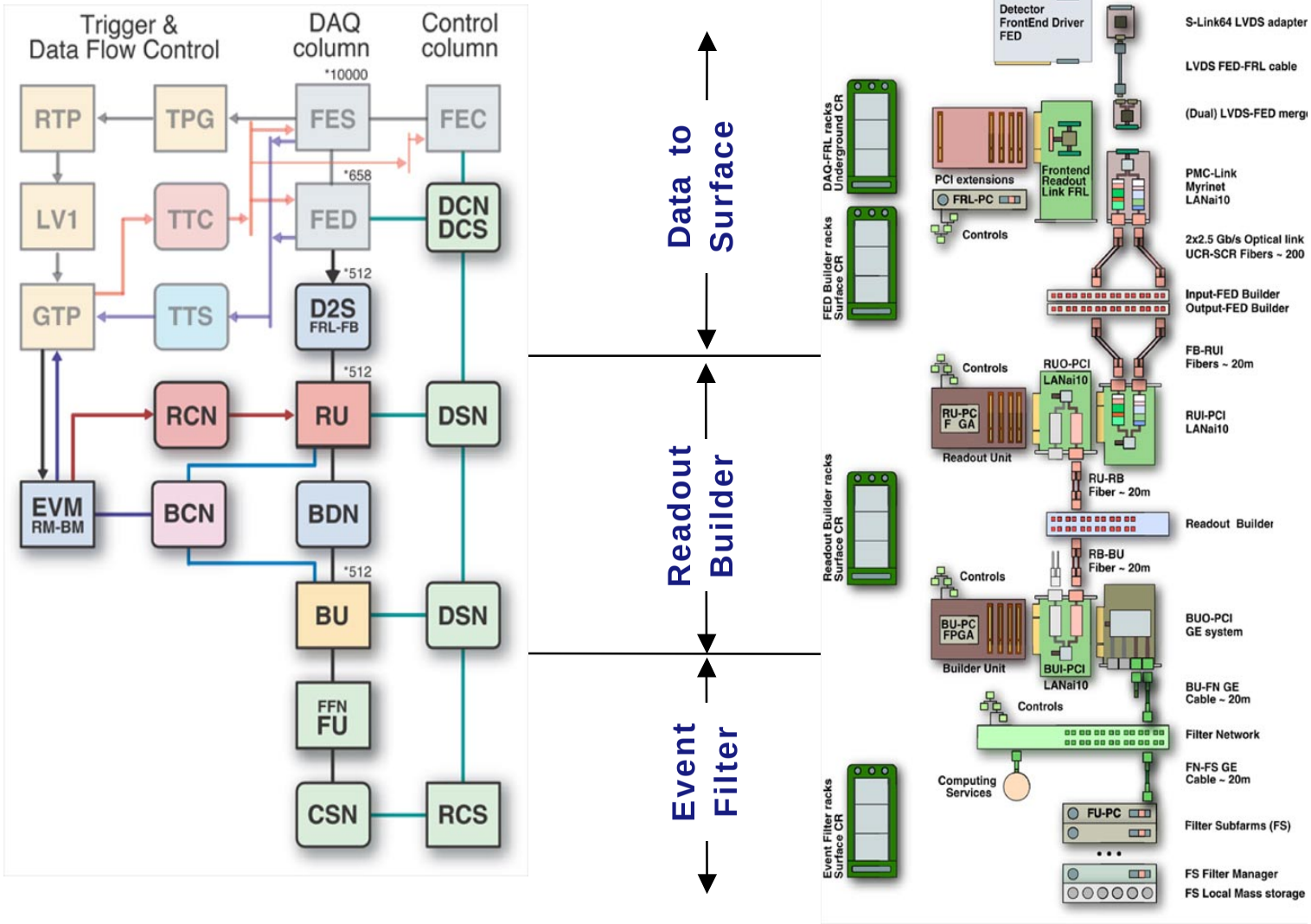




Detector readout to surface

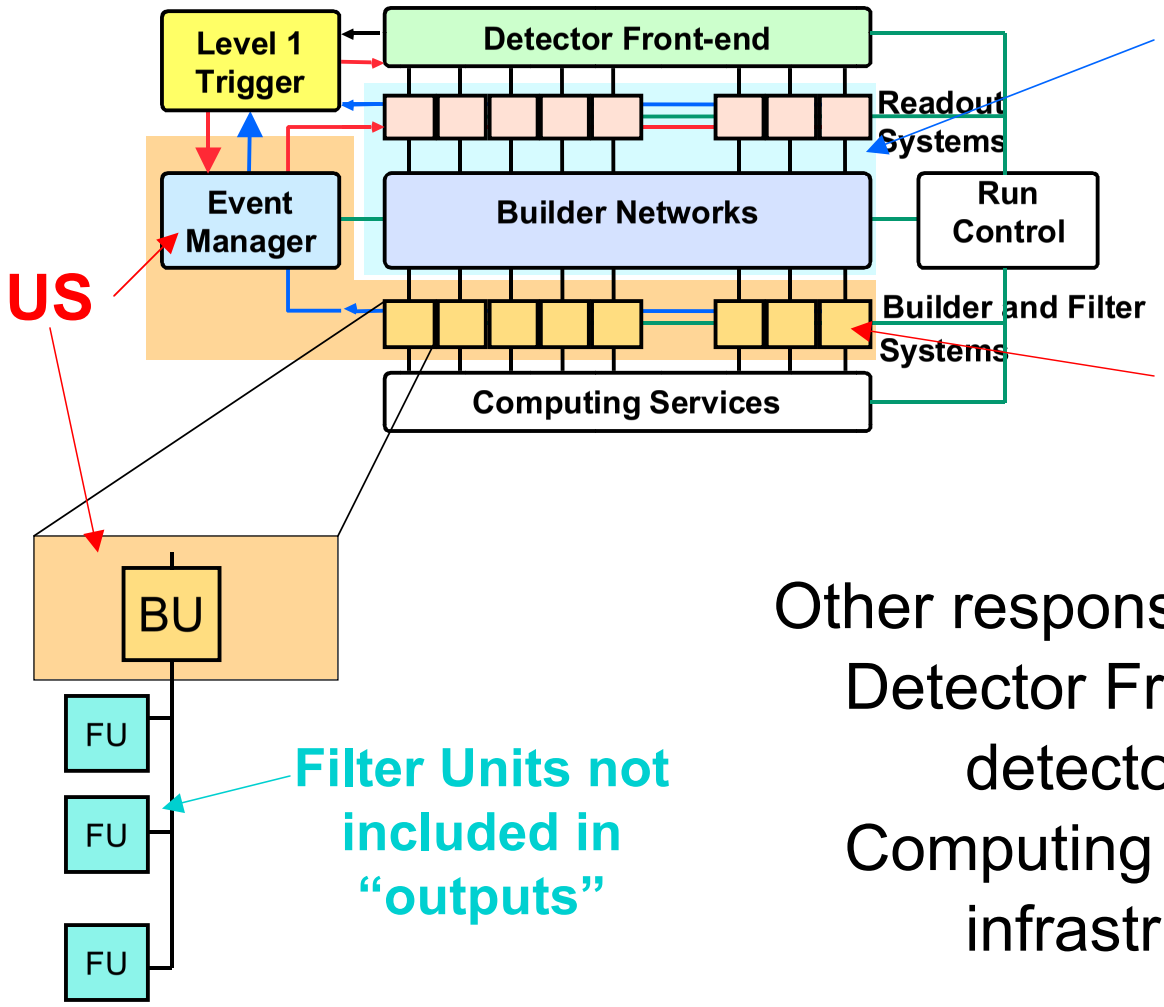


D2S + RB + EF breakdown



DAQ: US contribution (old)

US: Event Manager + Builder Units



CERN: Inputs(500) + Switch

US: Outputs + EVM

Filter Units not included in "outputs"

Other responsibilities:
Detector Front-Ends: detector groups
Computing Services: infrastructure

US contribution: new

Cover one segment (1/8) of the CMS DAQ plus _ of the Data-to-Surface system (plus the associated prototypes – "preseries")

- **Segment: 1 Readout Builder + 1 Event Filter**
- **US_CMS detector electronics is ~1/4 of the total**
- **Delivery of the system can be accomplished by the end of the US_CMS project (FY05)**
- **Aids the experiment most in the current phase where cash flow is very tight**
  - US R&D program can remain ~ unchanged (to the extent that the basic modules are the same)

Roughly speaking, the US

(a) works on/delivers prototype system (to 2004)

(b) delivers the "startup DAQ" for CMS (2005)

Milestones*

Prototype DAQ (US Contribution)

D2S Prototype	July, 2004
"Slice Test"	November, 2004 (*)
Readout Builder Prototype	April, 2005

Startup DAQ (US Contribution)

Filter Farm Ready	May, 2006
Readout Builder Ready	August, 2006

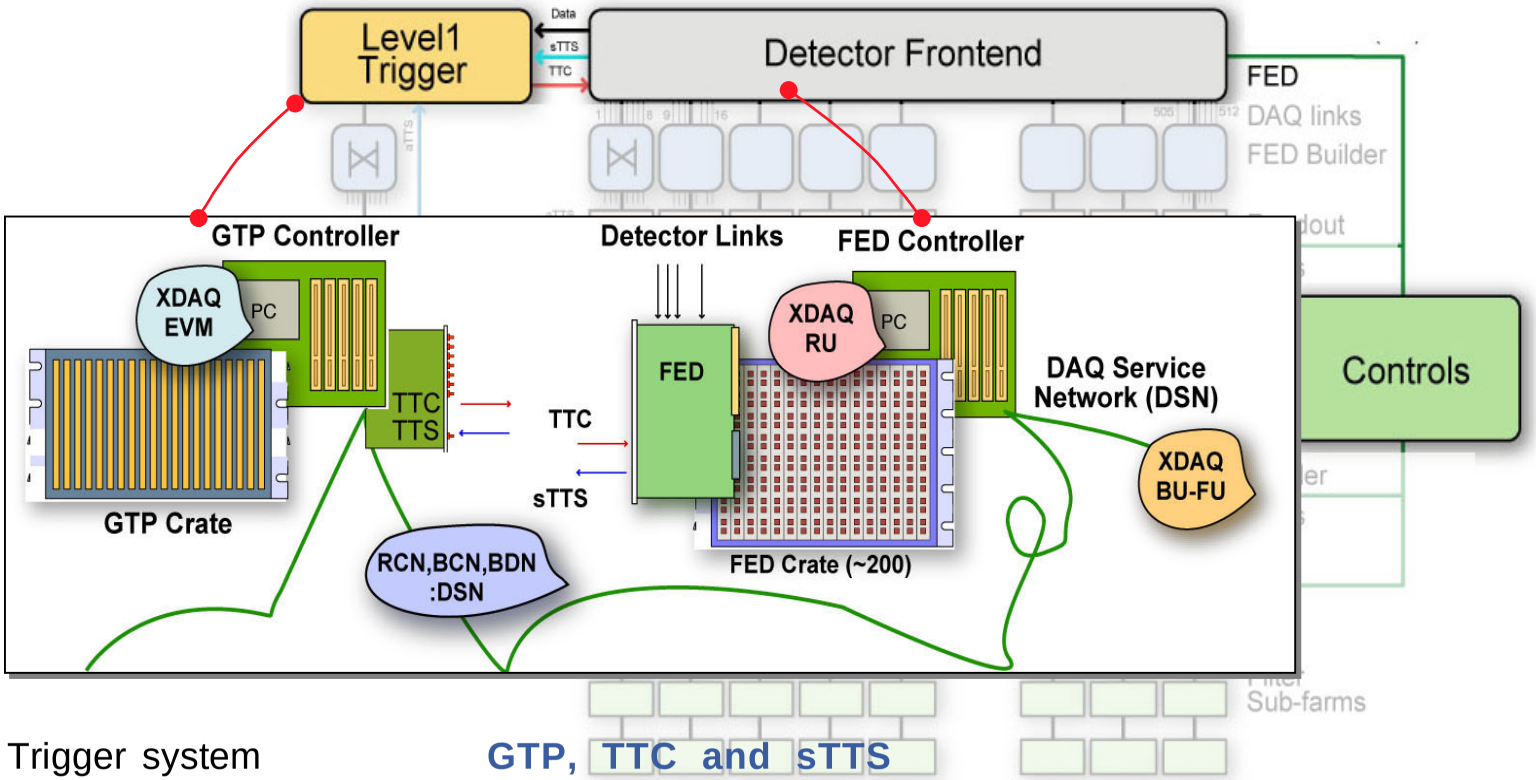
Declaration of Completion (US Contribution)

Startup DAQ ready for beam	September, 2006

(*) "Slice" Test for US-CMS detectors – DAQ will have full D2S proto + a few RB elements

*(Version 33)

Slice Test DAQ (10-100 Hz)



Trigger system	**GTP, TTC and sTTS**
Detector readout	Complete **FED crate systems** (FED-TTC-TTS, Controller CPU+DSN)
Readout Units	XDAQ **RU-VME-tasks** running in all the **FED controllers**
Data to Surface	None just the **FED-VME bus** of FED crates
RCN, BCN, BDN networks	DAQ Service Network (**DSN** e.g. GEthernet)
Event manager	XDAQ **EVM-task** running in the **GTP controller**
Builder/Filter Units	XDAQ BU-task running in **any DSN(WAN) CPU**
Performances	**Few 10 Hz (up to 100s when using GE switches in DSN as EVB)**