DØ Note 3599

THE INPUT DATA FLOW TO L2 STT TRIGGER CARD FROM SMT FRONT-ENDS

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Silvia Tentindo-Repond and Brian Connolly

Florida State University

Abstract

We review the existing information about data inputs to the L2 STT trigger card coming from the SMT front end. We specify the data flow from the SVXII chips to the L3 and MCH, through the SEQUENCER , the VRB and VBD path. We focus on the data flow after the SEQUENCER through the passive splitters to the VTM and then to the STT trigger card, and we define the consequent format of the data buffer to STT. The finality of this study is to provide the FPGA Cluster Finder in the L2 STT Trigger Card with the needed input specifications.

I. *GENERAL*

The STT preprocessor in Level 2 receives input from two separate streams: the data from the Silicon Microstrip Tracker detector (SMT) AND the data from the Fiber Tracker (CFT) Level 1 Trigger. Both inputs are needed for STTpp to be able to accomplish the task of associating 'tracks' seen in the SMT detector with tracks reconstructed in the CFT. Of course the STT must reconstruct SMT 'tracks' first, by finding hits and clusters and fitting them into tracks.

We concentrate on the data stream coming from the SMT detector, our primary task being to design and make operational the Cluster Finding Card in the STT Trigger Card, that needs these data as input to calculate hits and clusters.

II. *DATA FROM THE SMT DETECTOR INTO SEQUENCER*

Data from the SMT detector are collected at the Front End in SVXII chips. Data from each silicon ladder come in 8-bit words of channel address and channel signal alternated. There are 128 channels per SVXII chip. If the SVX is in 'zero-suppress' mode, only channels above pedestal are read out. Data from SVX are sent to a SEQUENCER via copper cable. There are 8 copper cables per SEQUENCER, and, per each cable, data are sent in form of 8 bit words every 18 ns (53 Mb/s). Each cable accepts data from 3 to 9 chips maximum. During the readout (Ref.1) of the SVX chips, the 8 bits of data from each of 2 HDIs (flexible circuit on which chips are mounted) is strobed into the FIFO memories of the SEQUENCER, and almost immediately readout into a G-Link Transmitter chip. The FIFO memories accept only 16 bit data. Into the G-Link trasmitter, data are serialized from 16 bit to 1 bit, and the resultant serial signal is fed into a laser optical driver, at a rate of 1.062 Gb/s (16 * 53 Mb/s), and from there data are sent to the VRB.

III. *SEQUENCER CARDS*

The SVX SEQUENCERs (Ref.1) make up the interface to the SVX chips in both the Silicon detector and the Fiber Tracker. They receive commands derived from the Serial Command Link and form the control signals necessary to run the SVX chips, moreover they route the data to the VRBs in the Counting House. There will be about 140 Sequencers in a total of eight crates located in the detector platform. Since they are located in an interlocked area, special diagnostic features are designed to isolate problems.

IV. *GENERAL BLOCK DIAGRAM FOR DATA FLOW TO L3 AND MCH*

```
                                  1 Gb/s
/------\                         |
| HDI  |__                       |
|      |  |                      |
\------/  |                      V
          |
          |  8 bits    16 bits     1bit
/------\  |          /---------\               /--------\
| HDI  |  -----------|SEQUENCER|_______________| VRB    |___
|      |-------------|         |               |        |   |
\------/             \---------/               \--------/   |
   .     TOTAL:                  TOTAL:            |        |
   .     8 copper cables        4 optical fibers   |        |
   .                                               |        |VME
   .                                               |        |backplane
                                               /--------\   |
                                               |  VBD   |___|
                                               \--------/
                                                   |
 TOTAL:                                            |data cable
 4 pairs of HDI's                                  |
 ( one HDI = 3 to 9                                |
           SVXII chips)                        /-------\
                                               |   L3  |
                                               \-------/
```

V. *DATA FROM SEQUENCER TO L3*

A 160 ft fiber carries the signal out the front panel of the SEQUENCER card and to the VRB's in the MCH (Moving Counting House). Four such links emerge from each SEQUENCER, each VRB accepts four fiber links. The data stream recovered by the VRB consists of 8 bit words IN SUCCESSION. A VME Backplane connects the VRB (VME Readout Buffer) and VBD (VME Buffer Driver). Data are then sent via cable to L3 and from there to permanent storage.

VI. *DATA STRUCTURE TO L3*

Every component in the data flow adds one Header into the structure of the data buffer: SEQUENCER Header, VRB Header, VBD Header. At the end of the data of each SEQUENCER there is also a SEQUENCER Trailer.(It is needed for reasons that we will discuss later; see VTM card).

Note that the "Channel" in the VRB Header refers to the 8 'Channels' i.e. copper cables that are fed into each SEQUENCER, wherever "CH" in the Chip 1, Chip 2, etc. buffers refers to the real ADC channels in the Silicon detector

```
                         \    VBD  Header
                         /
Word Size                \
   00                     |
Event #                   |
Status 0                  |
Status                    |
Channel 0 Byte Count      |   VRB Header
  "     1  "    "         |
  "     2  "    "         |
```

```
 "     3   "   "          |
 "     4   "   "          |
 "     5   "   "          |
 "     6   "   "          |
 "     7   "   "          /
SEQ ID                     \      Sequencer Header
HDI & SEQ STATUS           /
CHIP ID          \
   00             |
CH=03             |   Chip 1
 DATA             |
CH=5C             |
 DATA             /
 CHIP ID         \
    00            |
 CH=0             |
  DATA            |
 CH=1             |    Chip 2
  DATA            |
 CH=7E            |
  DATA            |
 CH=7F            |
  DATA            /
  C0                          \   Sequencer trailer
  C0                          /
```

A. *SEQUENCER's Data Readout HEADER*

The SEQUENCER ID is a number from 0 to 255; there will be 140 total SEQUENCERS in the detector. After the Sequencer ID, the next byte is defined, starting from the MSB (Most Significant Bit), as follows:

```
Downloaded Status bit 2
Downloaded Status bit 1
Downloaded Status bit 0
Control Link No_Synch
Control Link Parity Error
HDI #  bit 2
HDI #  bit 1
HDI #  bit 0
```

The Downloaded Status bits are provided for general use and are set via 1553. The three HDI # bits are numbered 0-7 and are associated with the cables connecting to the HDI interface Modules as follows:

```
0   A   half of top   cable (WRT Sequencer Backplane)
1   B    "       "       "
2   A    "      second  "
3   B    "        "      "
4   A    "       third  "
5   B    "        "      "
6   A    "       bottom "
7   B    "         "     "
```

B. *SEQUENCER's Data Readout TRAILER*

The Trailer for each HDI data stream will be hex C0 and will be appended to the data immediately, following the last data byte of the last chip on its HDI. The forced readout of channel 127 of the last chip on each HDI (a feature of the SVXII chip) will not be used; the option to use this feature, however,still exists. It is also assumed that no chip will ever have ID=C0.

C. *REMARK*

The information we are interested from sect.VI.A and VI.B is limited to the HDI # .

D. *REMARK*

In the VRB Header, the Word Size specifies the number of bits per word (8, 16 or 32). In the same VRB Header, the Event # information is provided to the VRB by the Serial Command Link. Note that this info will probably be provided by the SCL and to all the components of the Trigger System.

VII. *DATA TO L2 STT TRIGGER CARD*

When data come out of the SEQUENCER, passive splitters in the fibers allow the signal that goes to the VRB to be trasmitted to a VTM (VME Transition Module), and from there to the L2 STT Trigger Card. (Ref.2). The data are digitized into a FIFO whenever they are received by STT and are made ready for the Cluster Finder based on an FPGA processor that will process the data.

VIII. *GENERAL BLOCK DIAGRAM FOR DATA FLOW TO L2 STT*

```
 8 bits            16 bits     1 bit


/------\         /---------\                 /--------\
| HDI  |_________|SEQUENCER|_________________| VRB    |
|      |         |         |                 |        |
\------/         \---------/      |          \--------/
                                  |              |
                            /---------\
                            |  VTM    |
                            |         |
                            \_________/
                                 |
                                 |
                             /--------------------\
                             |  STT Trigger Card  |
                             |                    |
                             | /------------\     |
                             | |Cluster     |     |
                             | | Finder FPGA |    |
                             | \------------/     |
                             \____________________/
                                        |
```

IX. *VTM (VME TRANSITION MODULE)*

The role of VTM is to receive the serial data from the SEQUENCER and to convert them to a parallel form. Its function is also to transform the optical signal received from the SEQUENCER, through optical fibers, back to electronic signal. VTM feeds the 4 serial receivers to the J3 connector of the Backplane of the STT Card . In the data stream,the VTM reads the data buffer, looks for the SEQUENCER's trailer, and ignores all after that. (Ref. 3)

X. *DATA STRUCTURE TO STT TRIGGER CARD*

As already remarked, every hardware component in the data flow adds one Header into the structure of the data buffer: SEQUENCER Header, VRB Header, VBD Header.

In the data flow from SVX to STT, there is no VRB and no VBD Header. Besides, given the role of VTM, which is only a receiver, no Header is added by the VTM. So the final data structure seen as input to the STT Trigger Card is as follows:

```
SEQ ID                      \      Sequencer Header
HDI & SEQ STATUS            /
CHIP ID          \
   00             |
CH=03             |   Chip 1
 DATA             |
CH=5C             |
 DATA             /
 CHIP ID         \
    00            |
 CH=0             |
  DATA            |
 CH=1             |    Chip 2
  DATA            |
 CH=7E            |
  DATA            |
 CH=7F            |
  DATA            /
  C0                           \    Sequencer trailer
  C0                           /
```

Open questions: from where is the STT going to get the information of the Event number, Status, and Total bit number that is provided in the VRB Header for the Normal (to L3) data stream. ** The Sequencer's trailer could effectively be used for 'end of event', but we will probably need the Event # information anyway.

XI. CONCLUSIONS

The FPGA processor in the STT Trigger Card, will receive SMT data in the format described in sect.X of this report. The VTM module will provide them in the form of 16-bit words. From there on, the FPGA will process these data by applying a clustering algorithm (for example, see Ref.4) that will provide STT hits and clusters to the following units :

- the Track Fit Card in the L2 STT Trigger Card
- the L2 CFT preprocessor and
- L3

XII. *REFERENCES*

REF.1 - Mike Utes - "SVX Sequencer Board"
DO Engineering Note 3823.110-EN480 11/18/98

REF.2 - "A Silicon Track trigger for the DO Expt in Run II"
Proposal September 22,1998 . DONote 3516.

REF.3 - Mark Bowden, "VTM" private communication

REF.4 - Ulrich Heintz "Cluster Centroid Algorithm for STT"
28 Oct 98 . DONote 3421.