Fiber Road Card & L3 Buffering

H.Evans **Columbia U.**

FRC Tasks

1. **Communicate with SCL**
2. **Receive L1CTT Information**
3. **Distribute Trigger/Road Info to System**
4. **Control All Data Transfers to L3**
5. **Special VME Arbitration: VBD – CPU**

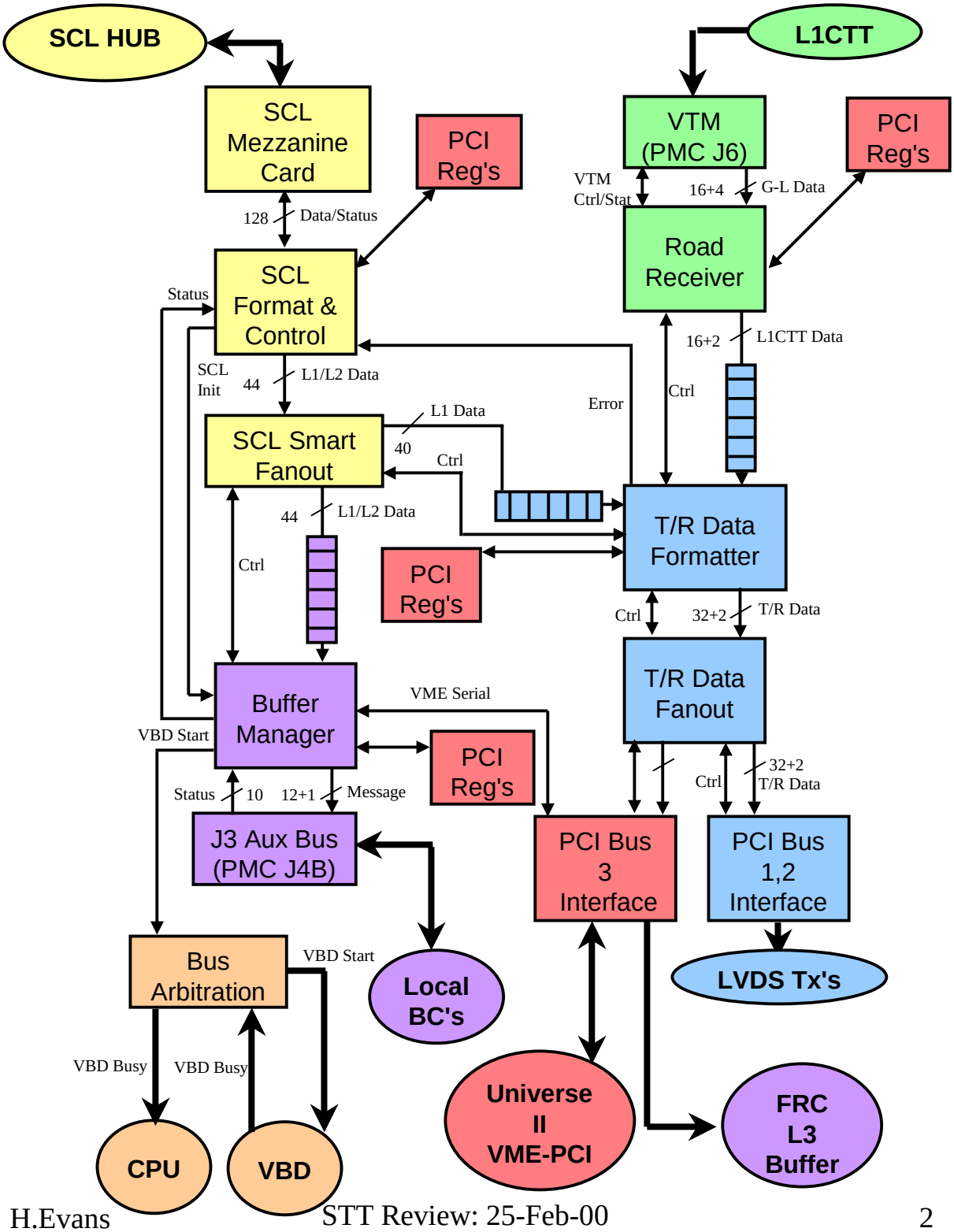
Implementation

- **PMC Daughterboard on Motherboard**
- **Modest FPGAs + FIFOs**

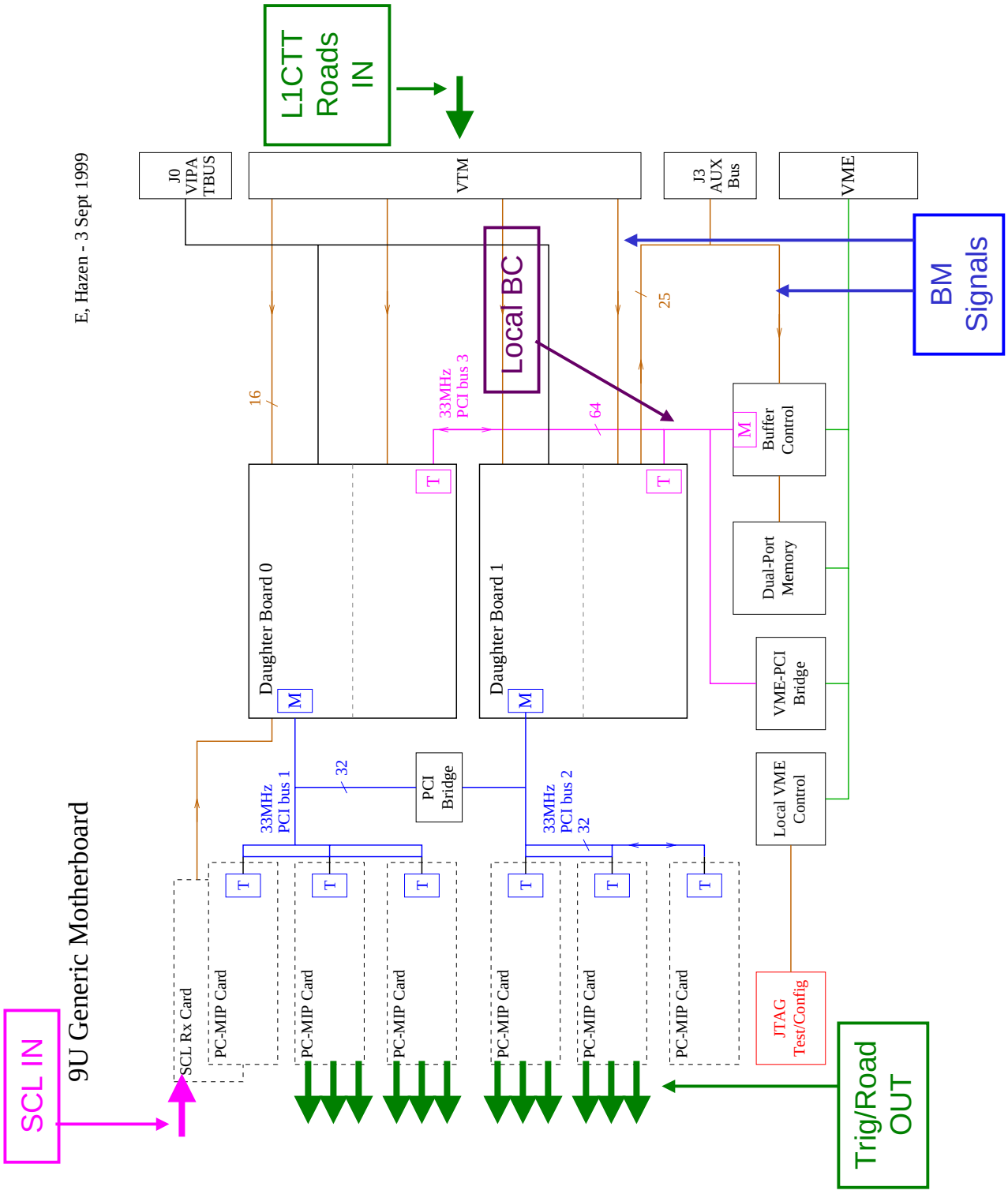
The Columbia/Nevis Team

- **Physicists:**
  - **Hal Evans (faculty)**
  - **Georg Steinbrück (postdoc)**
  - **Maurice Leutenegger (student)**
- **Engineers: Qi An, Bill Sippach**
- **Full Nevis Support**

FRC Functional View



On the Motherboard

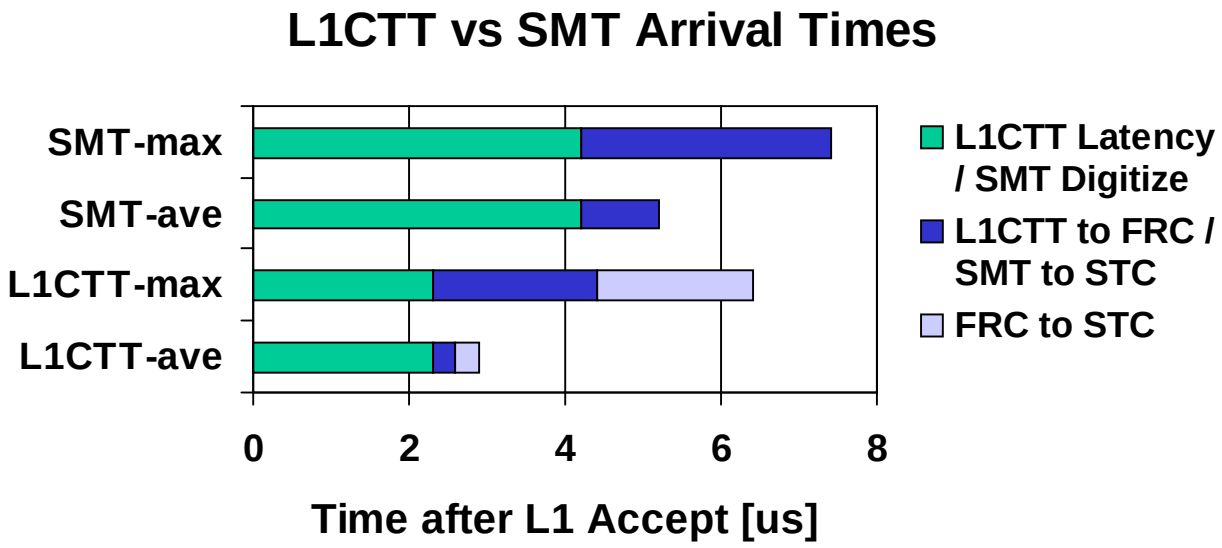


Communications Paths

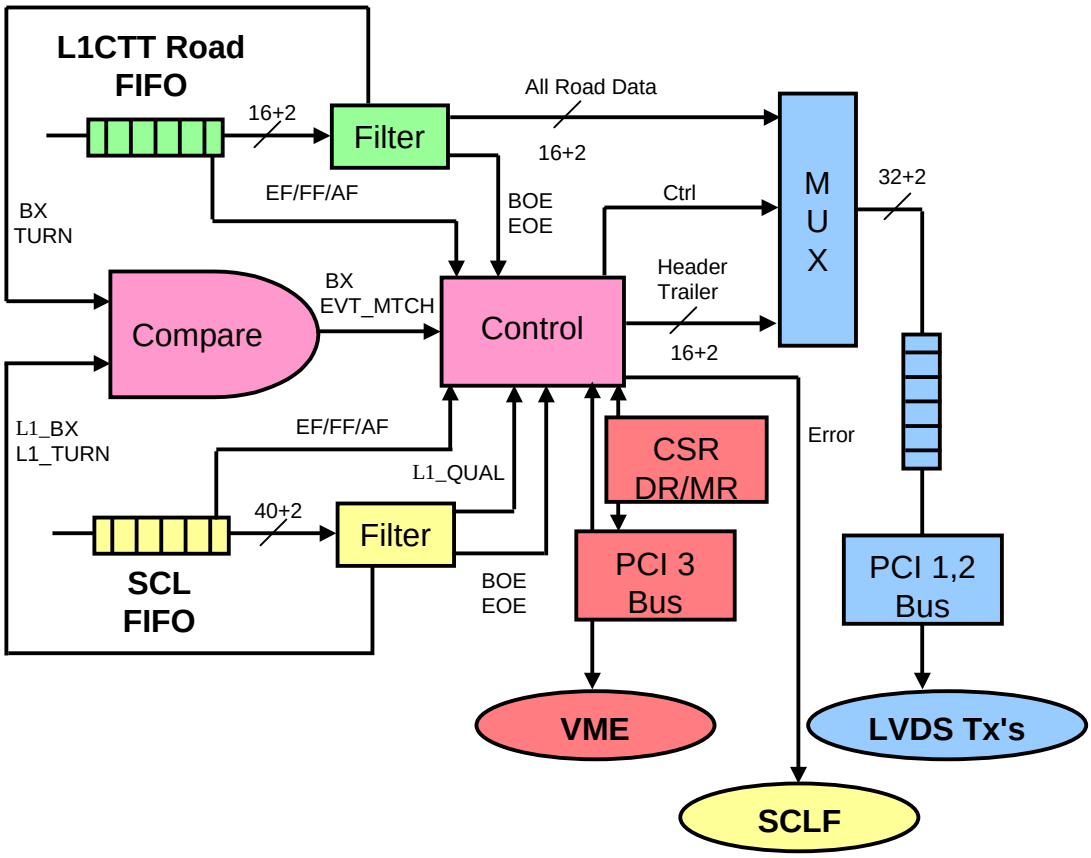
I/O	Data	Information	Src→Dst	Path
I/O	SCL	Trigger Error/Ack	Hub↔ Mezz ↔SCLF	MB0(J1,2) ↔PMC(J5,7)
I	L1CTT	Roads	VTM→RR	VTM→PMC(J6)
O	T/R Data	Trigger Info Roads	TRDF→LVDS Tx	PCI Bus 2
I/O	Buff Man	Buffer No.'s Status/Error	BM↔All BC's	J3 (~VRBC)
I/O	SCL Init	Init Req. Ack	BM↔All BC's	J3 (extra mess/stat)
I/O	Monitor	CollectStat	BM→CPU	Parallel port?
O	VME Arb	VBD Busy	BM→CPU	Parallel port?
I/O	L3 Start	VBD Collect	BM→VBD	J3 (slvrdy, done)
O	L3 Data	Indiv. Buff's	DB → BC →VBD	PCI Bus 3 VME

Timing

	Δt-min	Δt-ave	Action
L1 Decision	132ns	132ns	SCL→FRC
Yes	8.4μs	100μs	Data→STCs,TFCs BM→BCs (allocate)
L2 Decision	?	100μs	SCL→BM
Yes	?	1ms	BM→BCs (output)
Monitoring	132ns	132ns	SCL→FRC
Collect	?	~5s	FRC→Mon. Master



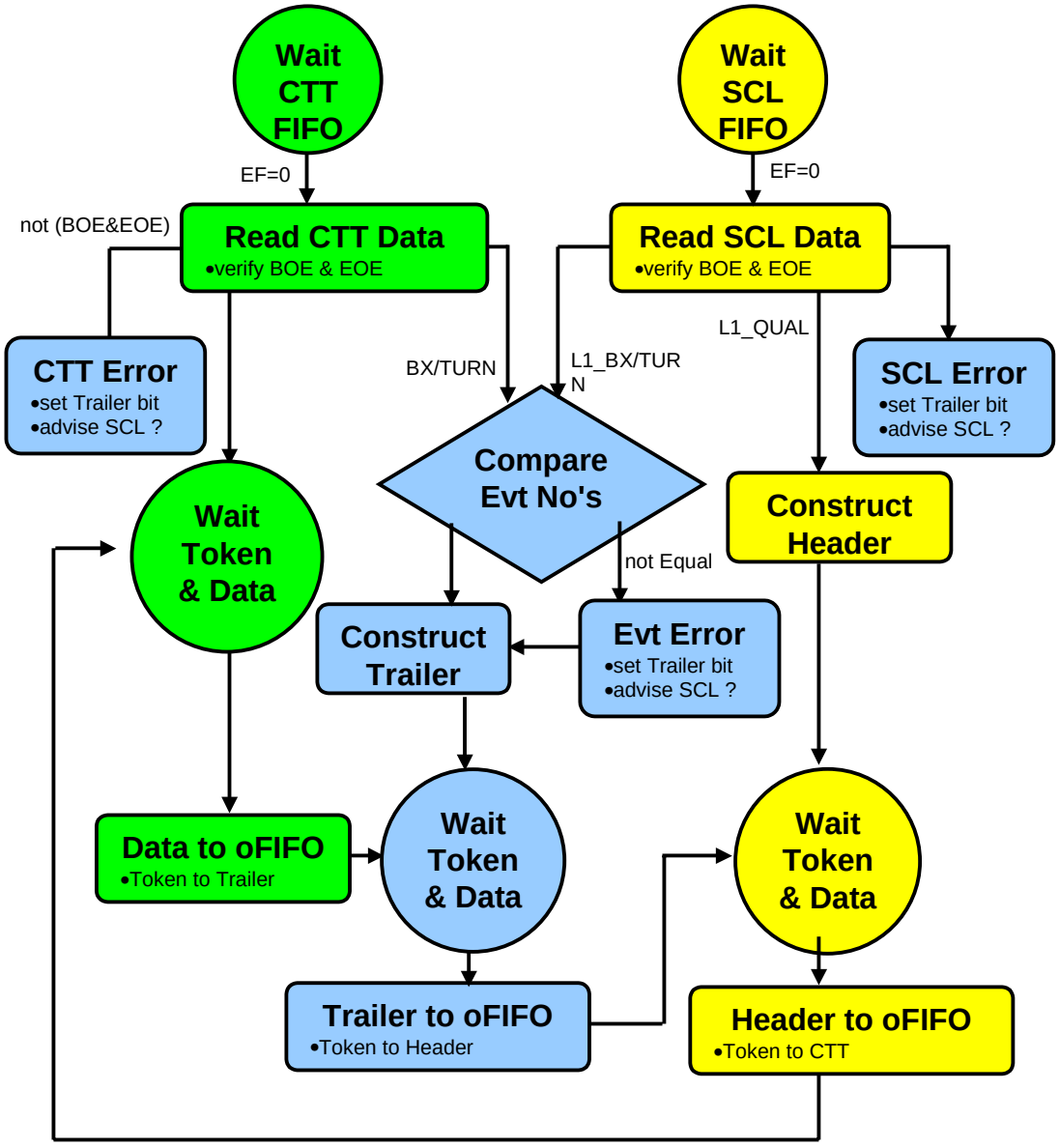
T/R Data – Block



Functions

1. **Event Synch** → **All Boards**
2. **Roads** → **STCs (assoc. hits)**
   → **TFCs (sent to L2CTT)**

T/R Data – Flow

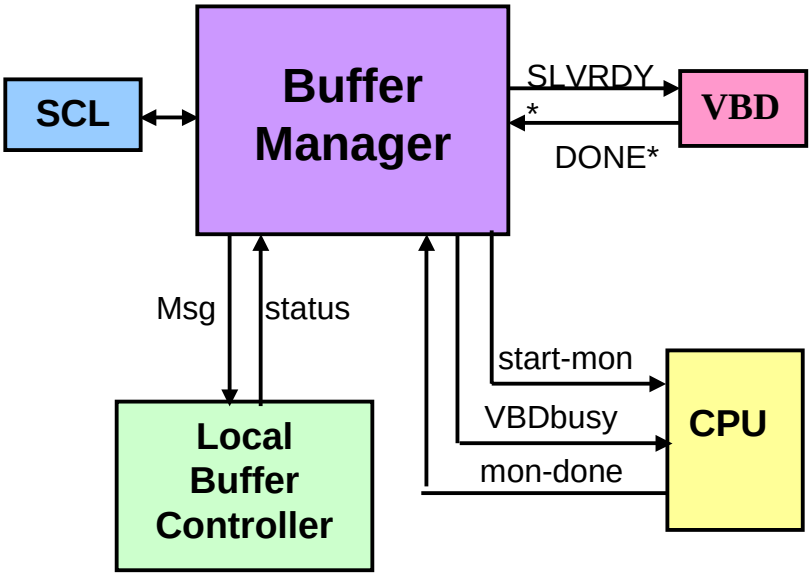

Wait CTT FIFO
EF=0
not (BOE&EOE)
Read CTT Data
•verify BOE & EOE
CTT Error
•set Trailer bit
•advise SCL ?
Wait Token & Data
Data to oFIFO
•Token to Trailer
Wait Token & Data
Trailer to oFIFO
•Token to Header
BX/TURN
L1_BX/TURN
Compare Evt No's
not Equal
Construct Trailer
Evt Error
•set Trailer bit
•advise SCL ?
Wait SCL FIFO
EF=0
Read SCL Data
•verify BOE & EOE
L1_QUAL
SCL Error
•set Trailer bit
•advise SCL ?
Construct Header
Wait Token & Data
Header to oFIFO
•Token to CTT

T/R Data Format

33	32	31 24	23 16	15 8	7 0
1	1	L1_QUAL		Link Tx	L1_BX
1	0	Head Length	No. Objects	Object Format	Object Length
1	0	L1_BX	Data Type	L1_TURN	
1	0	Algo min ver	Algo max ver	Status Bits	Firmware ver
1	0	P N Ntrk-Pt2	P N Ntrk-Pt1	P N Ntrk-Pt4	P N Ntrk-Pt3
0	0	S Pt 0	Err 0	Rel Φ 0	D Sector Addr
0	0	Data Type	L1_BX	Longitudinal Parity	
0	1	free		Link Tx Errors	L1_BX

- **Trigger Info**
  - L1 Qual — Processing Info for Event
  - BX/TURN — BX & Turn Numbers
- **Header**
  - P/N — Some Trks w/ Pos/Neg Pt
  - Ntrk-Ptx — No. of Trks in Pt Bin x
- **Data**
  - S — Sign of Trk
  - Pt Bin — Pt Bin Number (0-3)
  - Pt Ext. — Bin-1 (1.5-3 GeV) A-Offset
Bin-2 (3-5 GeV) A-Offset
Bin-3 (5-10 GeV) Pt-Info
Bin-4 (10- GeV) Pt-Info
  - Error — Transmission Errors
  - Rel Φ — H-Layer Fiber Number (0-43)
  - D — Track also sent to Adjacent Segm
  - Trk Adr — Address of 4.5° wedge of Trk

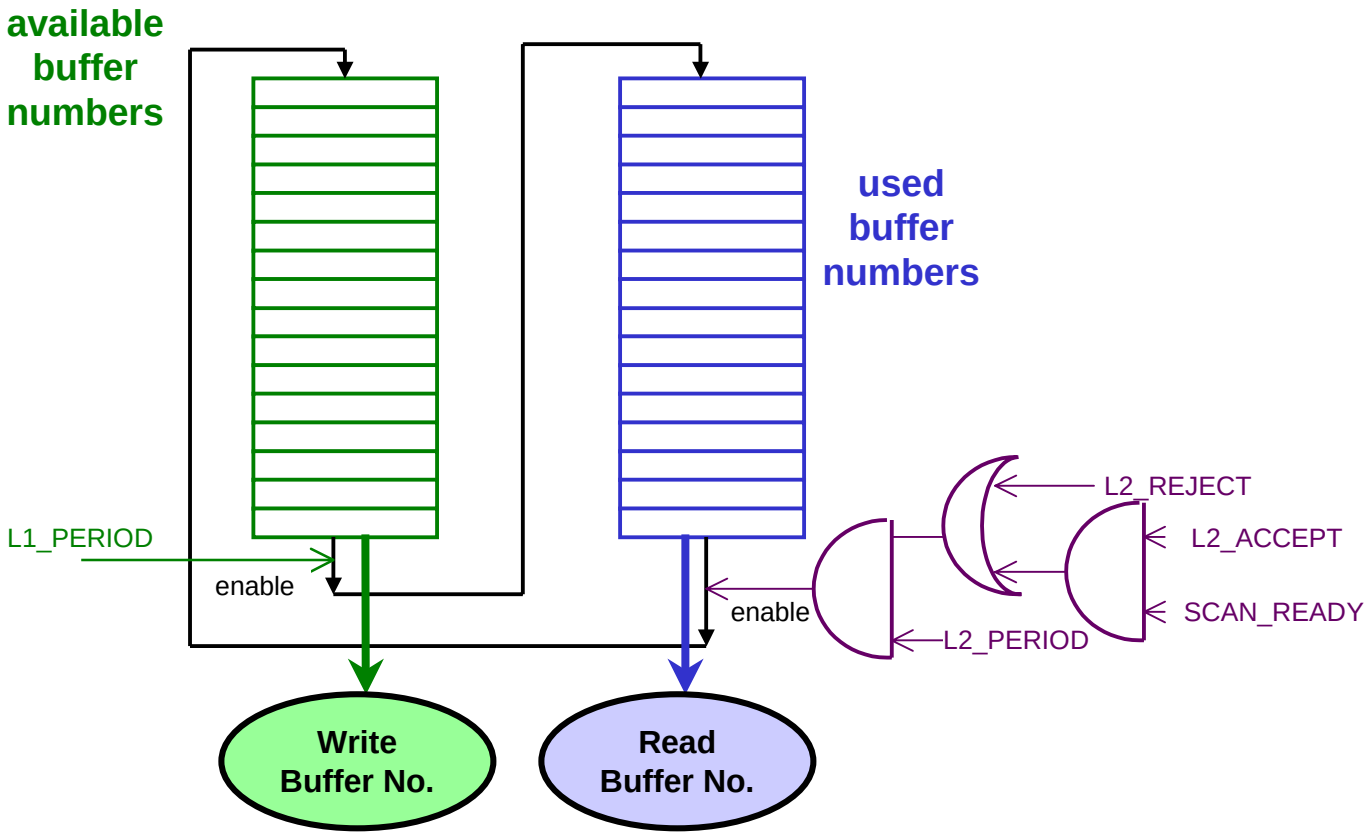
Buffer Management



Functions

1. Manage List of W/R Buffer No.'s for Entire System
2. Broadcast next W/R Buffer No. based on SCL Info
3. Receive Status Info from All Boards
4. Signal VBD to begin Reading Buffers
5. Signal CPU to begin Monitoring
6. Arbitrate VME bus between VBD and CPU
7. Broadcast SCL Init to Entire System
   - Receive Init Status from other boards
   - Send Init Status to SLCF → SCL Hub

Buffer Allocation

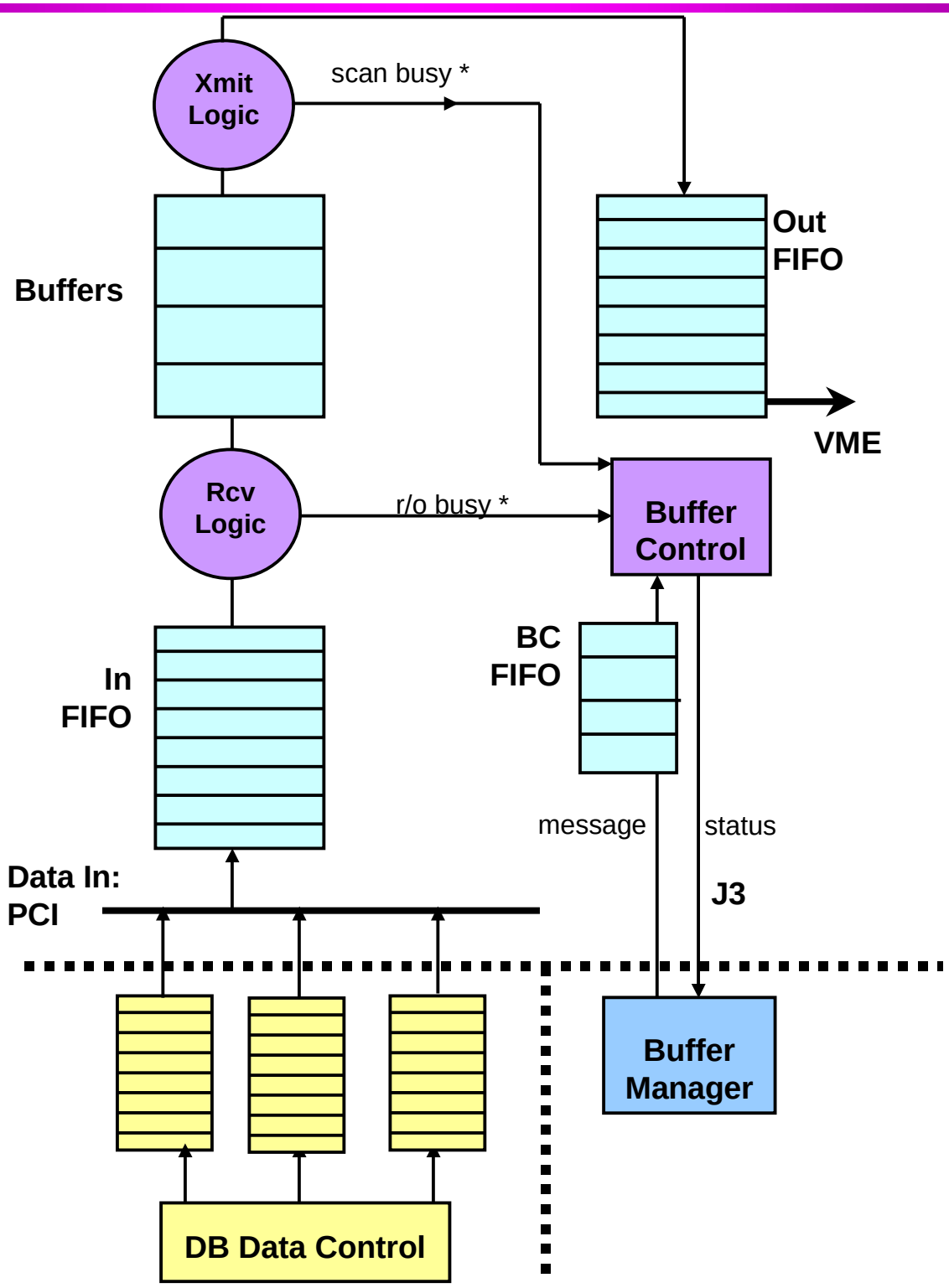


BM – Messages/Status

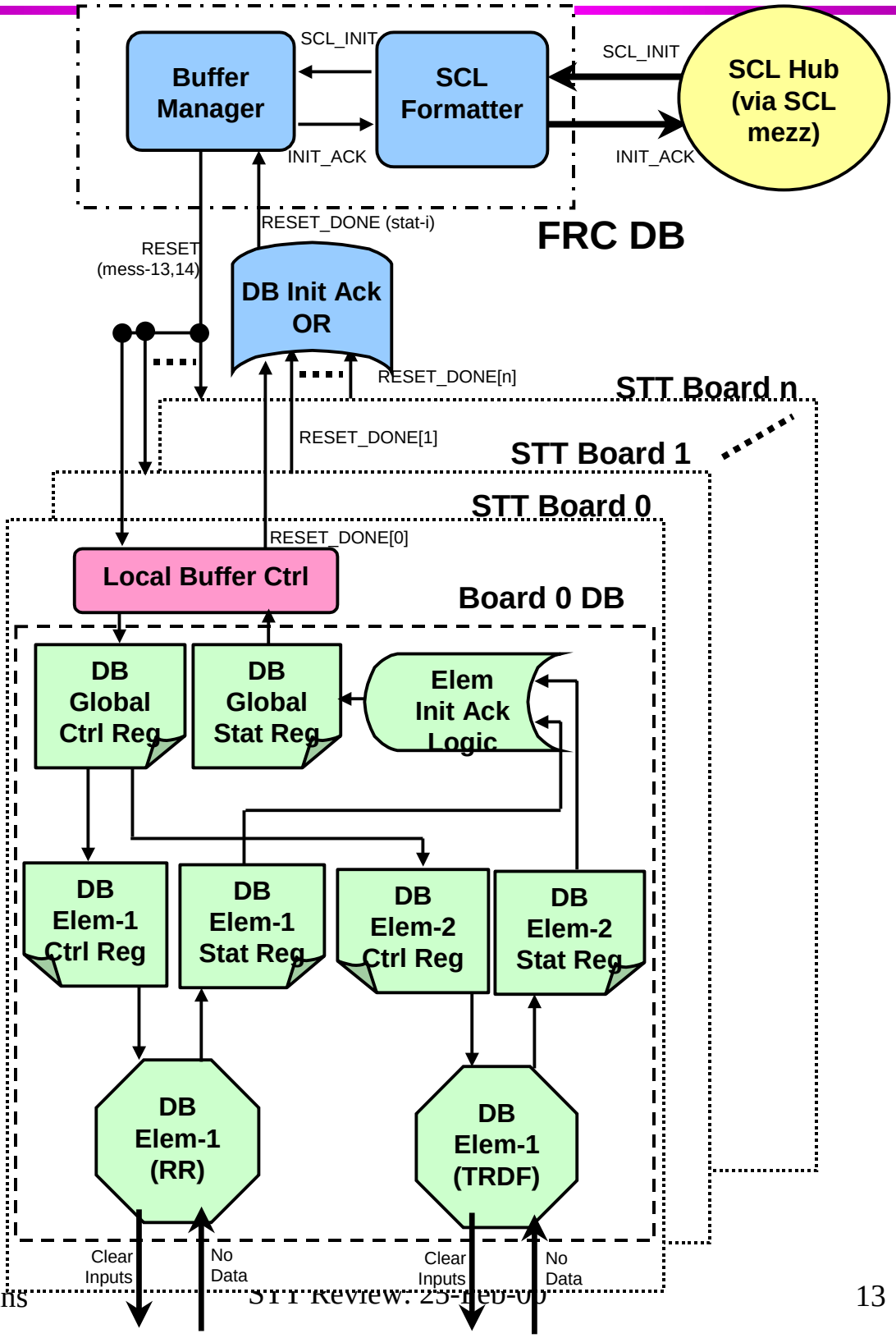
No.	Name	Purpose
	MESSAGES	
1	Readout Buffer No.	L1: next in buff no.
3	Bunch Crossing No.	L1: consistency
4	Scan Buffer No.	L2: VRB out buffer no.
5	Event No.	L2: event label
13	Clear Errors	clear errors - no reset
14	Reset/Restart	SCL Init (?)
	STATUS LINES	
0	Readout Busy	L1: in buffer busy
1	Scan Busy	L2: out buffer busy
2	Scan Ready	L2: Xfer$\rightarrow$out-fifo done
3	SCL Init Ack	Init Acknowledge
4	Init Done	Init Finished
5-9	free	Errors ???

Status Lines are ORed on Backplane

Local Buffer Controllers



SCL Init


Buffer Manager
SCL_INIT
SCL Formatter
SCL_INIT
SCL Hub (via SCL mezz)
INIT_ACK
INIT_ACK
FRC DB
RESET_DONE (stat-i)
RESET (mess-13,14)
DB Init Ack OR
RESET_DONE[n]
STT Board n
RESET_DONE[1]
STT Board 1
STT Board 0
RESET_DONE[0]
Local Buffer Ctrl
Board 0 DB
DB Global Ctrl Reg
DB Global Stat Reg
Elem Init Ack Logic
DB Elem-1 Ctrl Reg
DB Elem-1 Stat Reg
DB Elem-2 Ctrl Reg
DB Elem-2 Stat Reg
DB Elem-1 (RR)
DB Elem-1 (TRDF)
Clear Inputs
No Data
Clear Inputs
No Data

Testing/Monitoring

Monitoring

- **FRC Monitoring Data Size Small**
  - **Provide 256 Byte Monitoring Register for each element**

Testing

- **Simulated Data Flow Test**
  - **Require ability to load several events of data at each element in FRC**
  - **Small FIFOs (Data Register)**