Track Fitting Card

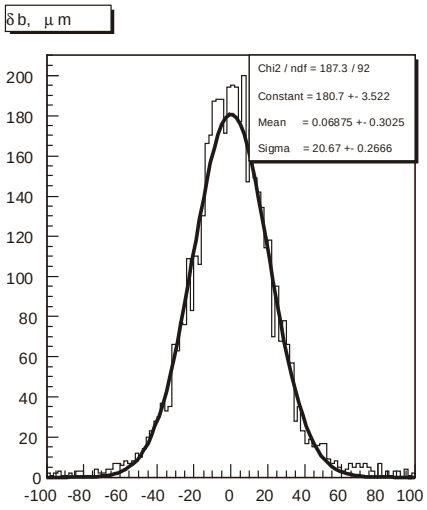
- Fit Algorithm
- Hardware Design
- Some numbers

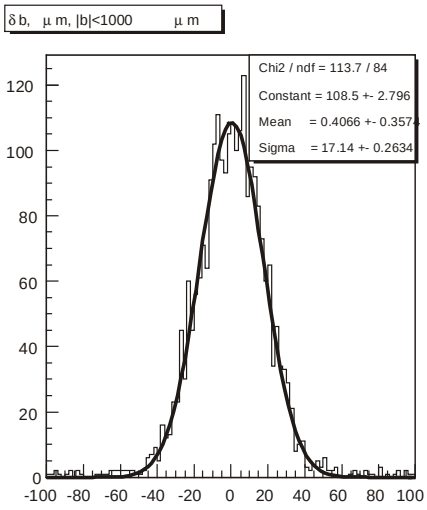
Fit Algorithm

- Two steps:
  - Hit selection (physics)
    - 4 layer detector, hits required in 3
    - hits closest to CTT (A,H) arc thru origin
    - one barrel transition allowed
  - Parameter Calculation (time)
    - Linearized $\chi^2 \Rightarrow p = M^*\phi$
      - p is 3-element parameter vector
      - M is $3x(N_{hit}-1)$ matrix depending on radii, resolutions
      - ϕ is $N_{hit}-1$ vector, $\phi_{hit} - \phi_c$
    - Twice: 4 layers tried, then 3 if bad χ^2.
- Asymptotic Resolution: 15-16 μm

Fit Algorithm, con't

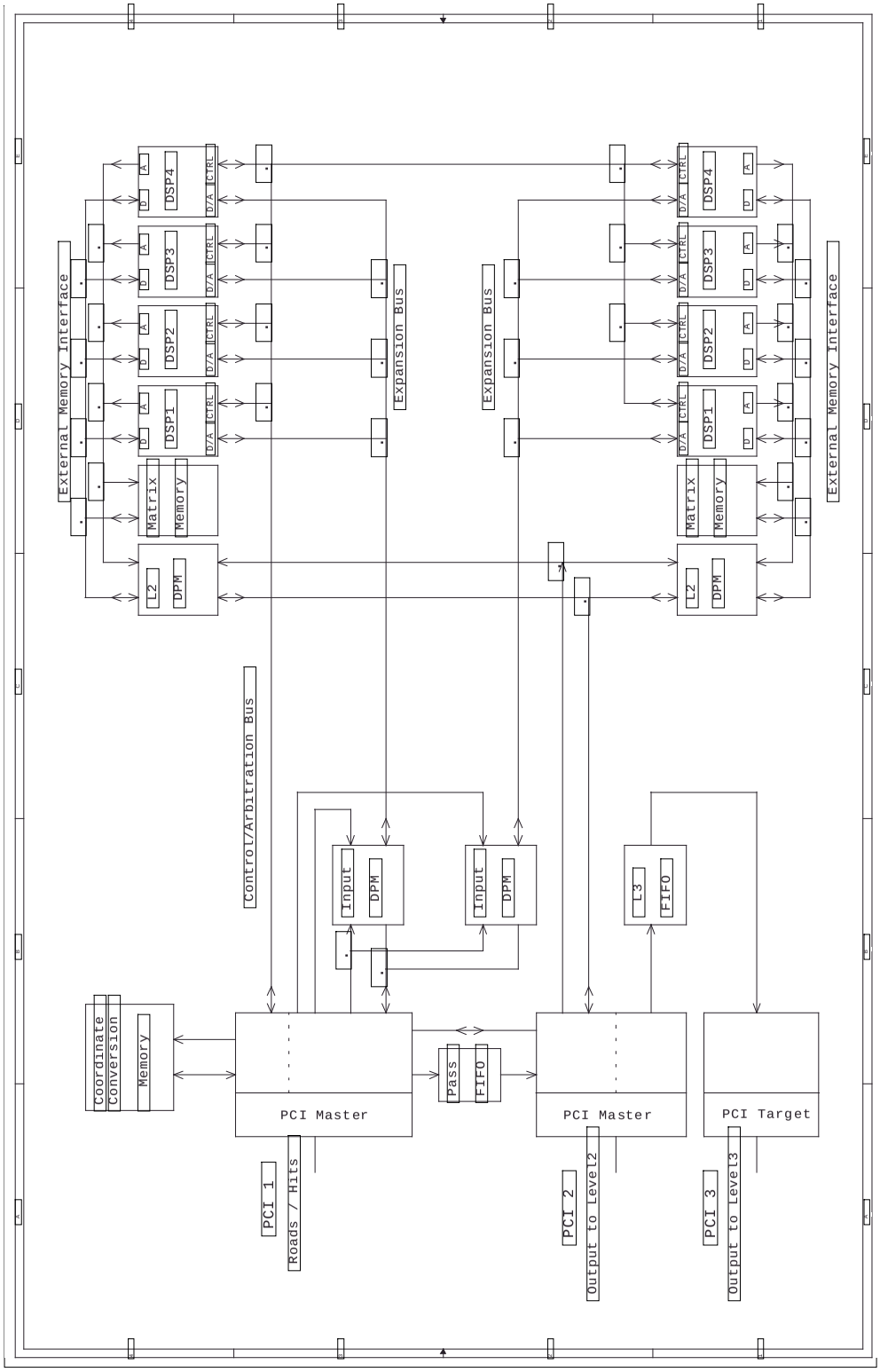
- Calculation details:
  - Integerized calculation
  - Matrices, M stored in look up
    divide azimuth into 80(?) superroads
    within each, matrices for different
      barrel ordering (-ve, +ve, crossing)
      sublayers used (Ignore overlap?)
      missing layer





  - LUT approx. 2 Mb
    Further refinement possible (size)

Block Diagram



Comments for block diagram:

Two cards per 60 degree sector
Each board is independent 30 degree sector
"Flow through" architecture
- Input and output on separate DSP buses
- Separate I/O controllers (352 pin FPGA's)
- Internal logical division into 2 processor sets
- Chosen TI6202/03 DSP's (small package!)

DSP input bus shared by four DSP's via DPM
DSP output bus shared by four DSP's via DPM

Can reuse DSP's trivially/event
Zeroth order initialization plan

Some numbers

- Timing (algorithm)

  1 pass: 7.4 + <1.5 (I/O) μs
  2 pass: 8.7 + <1.5 (I/O) μs

  - for 300 Mhz 6202/03
  - tested on 6701, scale by clock freq.
  - I/O contention: worst case, +5.8 μs
  - all data internal DSP memory except I/O buffers, Matrix LUT

- Cost:
  - $4000, major components
    $1000, boards, stuffing, …
- Power: 30 W
- Space: components only: 15-20%

L2STT Output

- Basic format
  - cannot fit into 32 bits (34, no errs)
  - 2 words: packing gives more precision than physics needs
- Transmit
  - TFC #1, L1CTT + L2STT (2 blocks*)
  - TFC #2, L2STT only
- What not packed CTT+STT format?
  - Empties: 30-40% at high lumi.
  - TFC's must intercommunicate or have additional filtering logic

Data Format

Word 1:

Bits 0-10: p_T (signed, p_T<100 GeV)
11-15: Spare
16-23: ϕ_0 (expand downward?)
24-28: χ^2
29: NSMT flag: 0, 3 layers;
1, 4 layers
30-31: dE/dx (3 bits instead?)

Word 2:

Bits 0-12: b, μm (signed, |b|<4 mm)
13-15: spare
16-21: CFT track index (0-41?)
22-23: spare
24-27: truncation in layer flags
28-30: barrel number
31: spare

Spares (11) will be zeroed?
Maybe send S_b as well?

Monitoring

- Collect_Status: Snapshot
  - processors states
  - processing time
  - cross check counters
  - overflow/mulitplicity info.
- Forced_Write/Unbiased
  - all input data (FRC+STC)
  - translated STC hit positions
  - Matrix LUT addresses
  - standard output data
  - collect_status data

Scalability

- Fit time is linear with multiplicity
  - Queueing sim.: no problems
  - Some algs. considered: non linear
- Additional hits
  - truncate STC output?
  - will truncate TFC input at 32/road
- Physics effects of 8-10 hits/layer?
- DSP offers maximum flexibility